8051 Core Flash MCU, 512 bytes SRAM, 8 Kbytes Flash ROM, 256 bytes independent EEPROM, 12-bit ADC, 8 channels of 16-bit PWM, 3 Timers, Multiplier-Divider, UART, SSI, CheckSum

1 General description

The SC92F5319/5312/5311/5310 series (referred to as SC92F531X) comprises enhanced 8051-core industrial Flash microcontrollers with an instruction set fully compatible with the traditional 8051 family.

The SC92F531X integrates 8 Kbytes Flash ROM, 512 bytes SRAM, and 256 bytes EEPROM. Up to 22 GPIOs, 12 external interrupt ports (which can be remapped to cover 22 I/Os), 3 independent 16-bit timers, 22+1 channels of 12-bit high-precision ADC, 8 channels of 16-bit high-performance PWM, 2 channels of conventional PWM (two outputs from Timer 2), an internal high-frequency 32 MHz oscillator with ±1% accuracy, a low-frequency 32 kHz oscillator with ±4% accuracy, 1 UART, 1 three-in-one serial communication interface which can be used as UART/SPI/TWI (SSI), a built-in LED driver supporting normal and bidirectional drive modes, and 1 integrated OP/CMP dual-function analog operational amplifier module. To improve reliability and simplify customer circuits, the SC92F531X internally integrates a 4-level selectable voltage LVR, built-in voltage references of 1.024 V, 2.4 V, and 2.048 V for ADC. The SC92F531X offers excellent noise immunity, making it well-suited as a main controller for diverse applications including smart home appliances, Internet of Things (IoT), wireless communications, gaming consoles, and various industrial control and consumer electronics fields.

2 Features

Operating conditions

- Operating voltage: 2.4 V to 5.5 V
- Operating temperature: -40 to 105 ℃

EMS

- ESD
  - HBM: JS-001-2023 Class 3A
  - CDM: ANSI/ESDA/JEDEC JS-002-2022 Class C3
- EFT
  - EN61000-4-4 Level 4

Package types

- 8-Pin: SOP8
- 16-Pin: SOP16
- 20-Pin: SOP20 / TSSOP20 / QFN20(3X3)
- 24-Pin: SSOP24 / QFN24(4X4)

Core: 4T 8051

- System clock supports up to 32 MHz, minimum instruction cycle 125 ns

Flash ROM

- 8 Kbytes Flash ROM
- Can be rewritten 1000 times

EEPROM

- 256 bytes EEPROM
- Can be rewritten 10,000 times
  - When the user writes to the EEPROM, ensure the V_{DD} range is between 2.5 V and 5.5 V

SRAM

- 256 bytes on-chip directly addressable RAM
- Additional 256 bytes on-chip indirectly addressable RAM
- PWM duty cycle setting RAM
- LED display RAM
- Port mapping RAM

Programming and debugging

- 2-wire JTAG programming and debugging interface: P1.2 / tCK , P1.3 / tDIO
- When programming the Flash ROM, ensure the 5V voltage level is selected

Built-in high-frequency 32 MHz oscillator (HRC)

- When used as the system clock source, the system clock frequency f_{SYS} can be set to 32/16/8/2.66 MHz via the programmer
- Frequency accuracy:
  - Operating across (2.4 V to 5.5 V) and in an application temperature range of -40 to 85 ℃, not exceeding ±1%
  - Operating across (2.4 V to 5.5 V) and in an application temperature range of -40 to 105 ℃, not exceeding ±1.5%

Built-in low-frequency 32 kHz RC oscillator (LRC)

- Can be used as the clock source for watchdog timer (WDT)
- Can be used as the clock source for the Base Timer and wake the device from STOP mode
- Frequency accuracy: operating across (4.0 V to 5.5 V) and at a room temperature of 25 ℃, not exceeding ±4%

Low voltage reset (LVR):

- Reset voltage has four selectable levels: 4.3 V, 3.7 V, 2.9 V, and 2.3 V
- Default setting corresponds to the Code Option value programmed by the user

Interrupts (INT):

- A total of 11 interrupt sources, including Timer0 to Timer2, INT0, INT1, ADC, PWM, UART0, SSI, Base Timer, and CMP
- External Interrupts:
  - Two interrupt vectors with 12 interrupt pins, each configurable for rising edge, falling edge, or dual-edge triggering
  - 12 external interrupt pins can be multiplexed into two groups, covering 22 I/O ports
- Supports two-level interrupt priority configuration

Digital peripherals:

- Up to 22 independent I/O pins with individually configurable pull-up resistors
- 8 ports from LED0 to LED7 share a single 16-level programmable constant current source
- LED0-LED7 ports can provide 130 mA @0.8 V high current sinking capability
- 11-bit WDT with selectable clock prescaler
- Three timers: TIMER0, TIMER1, and TIMER2
- TIMER2 is a multifunction timer supporting:
  - Capture function via T2EX
  - Two conventional PWM outputs: PWM20 and PWM21
  - PWM21 can be multiplexed to any I/O port
  - T2EX can be multiplexed to any I/O port
- PWM0: 8 channels of 16-bit PWM
  - Can be set to independent or complementary mode:
    - In independent mode, 8 PWM channels share the same period, duty cycles can be set individually
    - In complementary mode, four pairs of complementary PWM signals with dead time are output simultaneously
  - Output waveforms can be inverted and configured as center-aligned or edge-aligned
  - Supports PWM fault detection mechanism (FLT)
- One dedicated UART communication port
  - RXD0 and TXD0 can be independently multiplexed on any I/O port
- One three-in-one serial communication interface which can be used as UART/SPI/TWI (SSI)
  - The three signal lines of SSI can be independently multiplexed on any I/O port
- Built-in Checksum accumulator and verification module
- Integrated 16 ×16-bit hardware multiplier and divider

LED driver:

- A total of 8 LED driver pins: LED0 to LED7
- All LED pins support 16-level source drive control
- LED0 to LED7 driver pins can provide 130 mA@0.8 V high current sinking capability
- IC system clock is used as the LED clock source
- After each LED frame scan completes, the corresponding LED driver flag AUIF is set
- During automatic scanning, the output period width of SEG matches that of COM
- LED dead time is configurable
- Characteristics of the LED bidirectional drive mode are as follows:
  - LED0-LED7 support bidirectional drive mode, enabling simultaneous driving of up to 7x8 LED pixels
  - Eight selectable scanning modes available, ranging from “7 x 8” down to “1 x 1”
  - The COM function of any LEDn port can be disabled, making the COM port inactive during the scan cycle while preserving its function as a SEG port. This feature enhances the brightness of the LED array
  - Common pins LED0, LED1, LED6, and LED7, with four selectable scan times: 0.5T, 1T, 1.5T, and 2T

Analog peripherals:

- Integrated dual-function CMP/OP module
  - Configurable as analog comparator (CMP) or operational amplifier (OP)
  - CMP
    - Four selectable positive inputs
    - CMP comparison voltage can be selected from external input or a 15-level V_{DD} divider
    - Typical CMP response time: 2μs
    - Can wake the device from STOP mode
  - OP
    - One selectable non-inverting input and one inverting input
- 22+1 channels of 12-bit ADC
  - 22 external ADC input channels
  - One internal ADC channel can directly measure VDD
  - Built-in reference voltages of 1.024 V / 2.4 V / 2.048 V
  - The ADC reference voltage has four options: VDD and internal 1.024 V / 2.4 V / 2.048 V
  - Configurable ADC conversion complete interrupt

Power saving modes:

- IDLE mode, can be woken up by any interrupt
- STOP mode, can be woken up by INT0~1, BaseTimer, and CMP

92 Series product naming rules

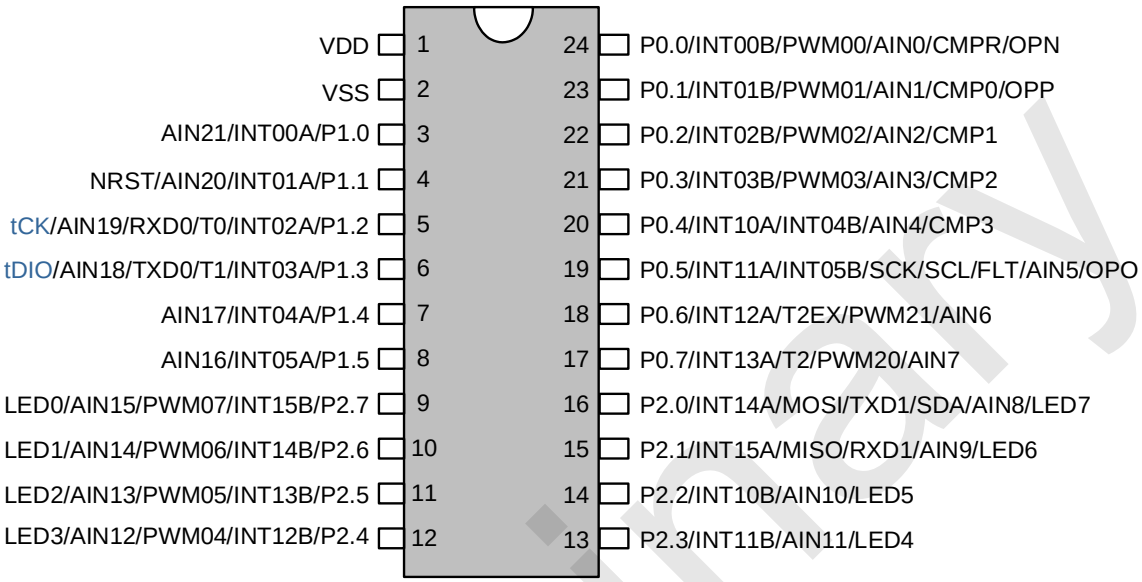
Name	SC	92	F	5	3	1	9	X	Q	24	R
Serial Number	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪

Serial Number	Meaning
①	SinOne Chip (abbreviation)
②	Product series name
③	Product Type (F: Flash MCU)
④	Serial number: 5: GP series, 6: TK series
⑤	ROM Size: 1 is 2K, 2 is 4K, 3 is 8K, 4 is 16K, 5 is 32K…
⑥	Sub-series number: 0-9, A-Z
⑦	Number of pins: 0: 8pin, 1: 16pin, 2: 20pin, 3: 28pin, 5: 32pin, 6: 44pin, 7: 48pin, 8: 64pin, 9: 100pin/24pin
⑧	Version number: (Default, B, C, D)
⑨	Package type: (D:DIPM:SOPX:TSSOPF:QFPP:LQFPQ:QFNK:SKDIP)
⑩	S:MSOP/SSOP
⑪	Number of pins

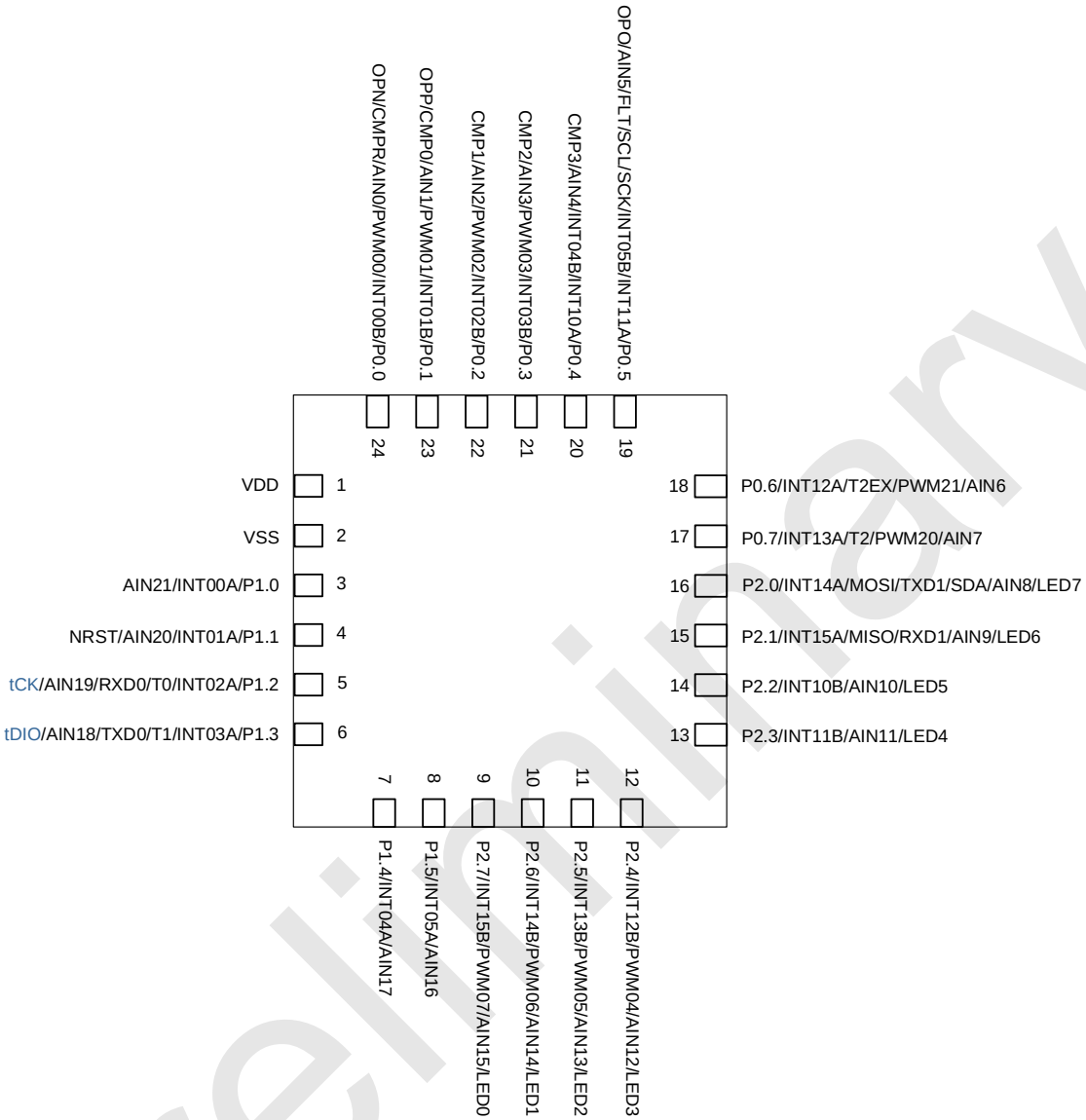
Catalog

3 Pin definition

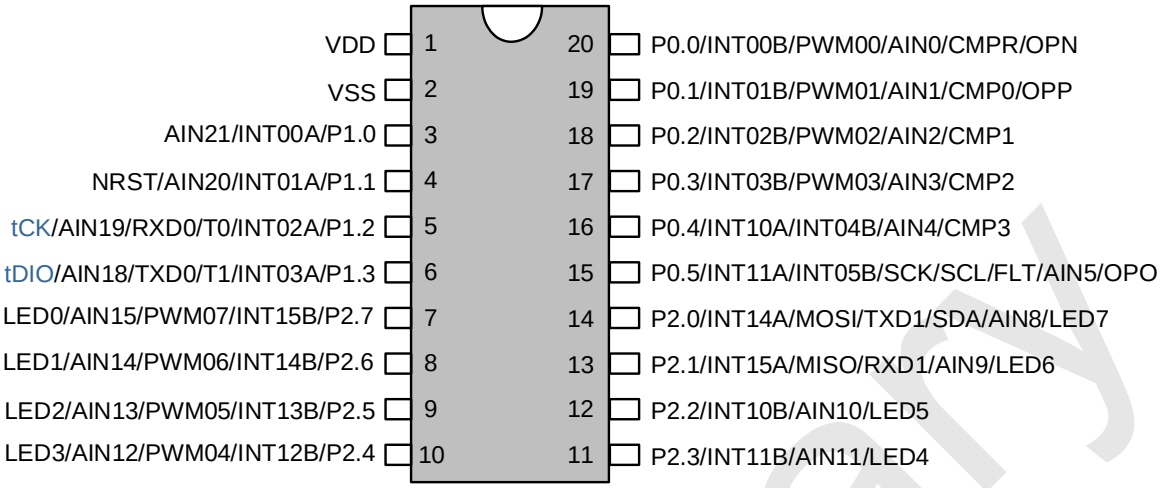
3.1 Pin configuration



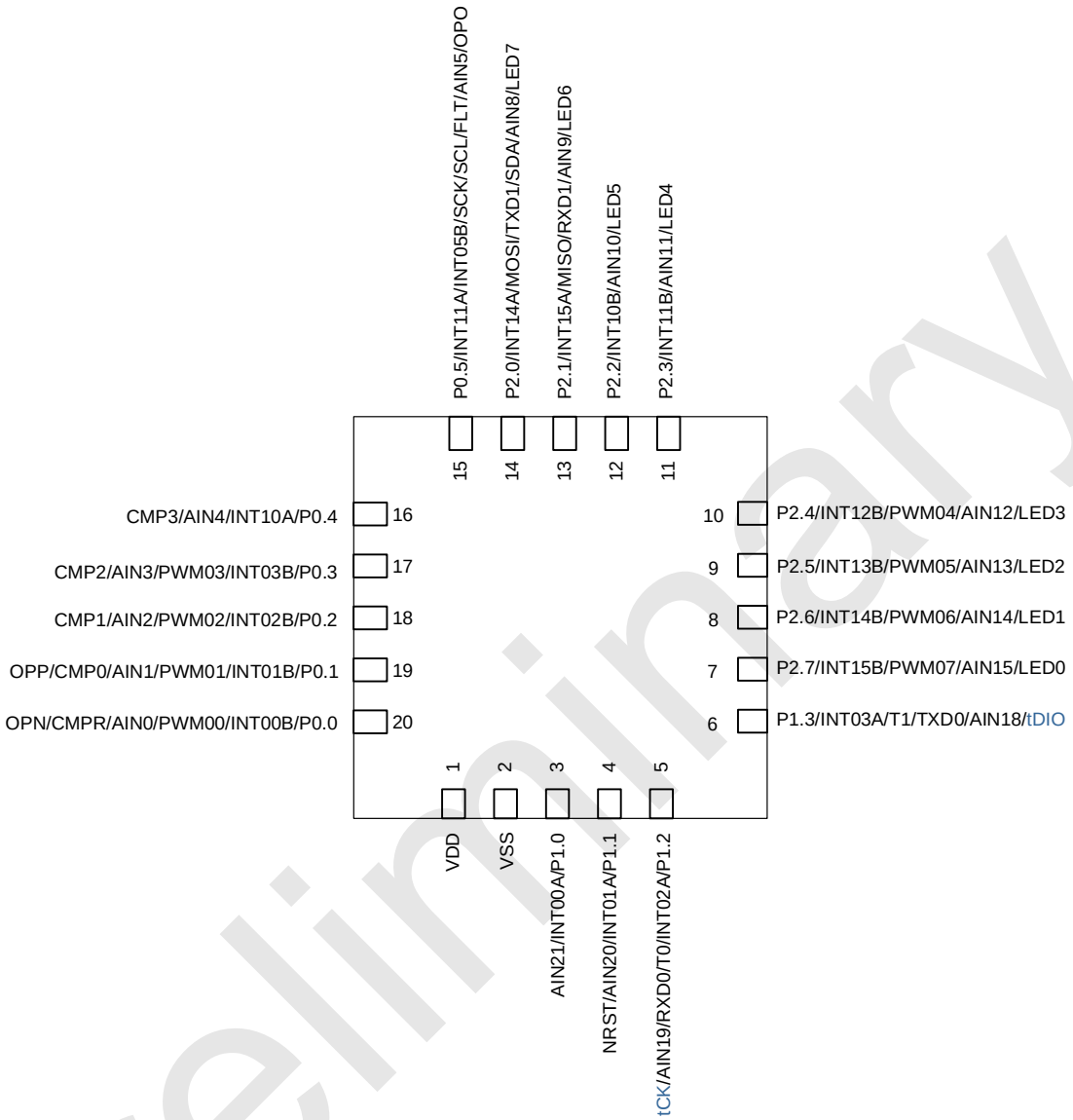
SC92F5319 pin configuration diagram
for SSOP24 package



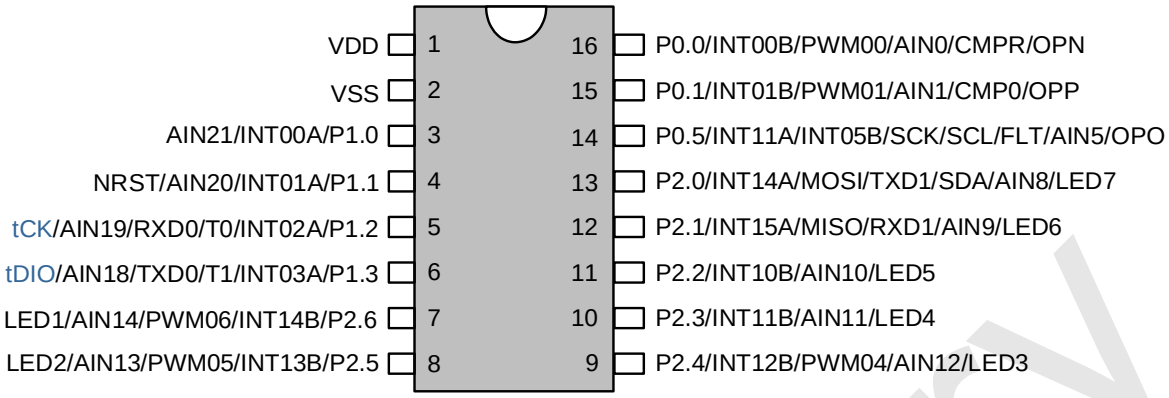
SC92F5319 pin configuration diagram
for QFN24 package



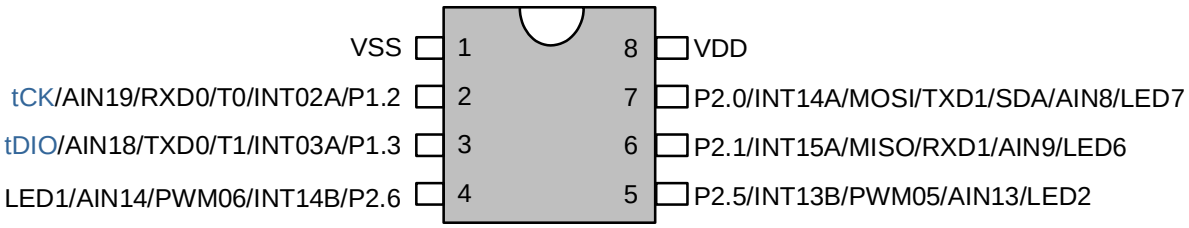
SC92F5312 pin configuration diagram
for SOP20/TSSOP20 package



SC92F5312 pin configuration diagram
for QFN20 package



SC92F5311 pin configuration diagram
for SOP16 package



SC92F5310 pin configuration diagram
for SOP8 package

3.2 Pin Definition

3.2.1 Pin resource list

Pin Number				Pin Functions												
SSOP24/ QFN24	SOP20/ TSSOP20 /QFN20	SOP16	SOP8	IO	Other	LED	ADC	CMP	OP	PWM0	SSI	UART0	TPWM	Timer	INTSEL =0	INTSEL =1
1	1	1	8	VDD												
2	2	2	1	VSS												
3	3	3	-	P1.0			AIN21								INT00A	
4	4	4	-	P1.1	NRST		AIN20								INT01A	
5	5	5	2	P1.2	tCK		AIN19				-	RXD0		T0	INT02A	
6	6	6	3	P1.3	tDIO		AIN18				-	TXD0		T1	INT03A	
7	-	-	-	P1.4			AIN17								INT04A	
8	-	-	-	P1.5			AIN16								INT05A	
9	7	-	-	P2.7		LED0	AIN15			PWM07						INT15B
10	8	7	4	P2.6		LED1	AIN14			PWM06						INT14B
11	9	8	5	P2.5		LED2	AIN13			PWM05						INT13B
12	10	9	-	P2.4		LED3	AIN12			PWM04						INT12B
13	11	10	-	P2.3		LED4	AIN11									INT11B
14	12	11	-	P2.2		LED5	AIN10									INT10B
15	13	12	6	P2.1		LED6	AIN9				SSIRX0 (MISO/RXD1)				INT15A	
16	14	13	7	P2.0		LED7	AIN8				SSITX0 (MOSI/SDA/TXD1)				INT14A	

Pin Number				Pin Functions												
17	-	-	-	P0.7			AIN7						PWM20	T2	INT13A	
18	-	-	-	P0.6			AIN6						PWM21	T2EX	INT12A	
19	15	14	-	P0.5			AIN5		OP_O	FLT	SSICK0 (SCK/SCL)				INT11A	INT05B
20	16	-	-	P0.4			AIN4	CMP3							INT10A	INT04B
21	17	-	-	P0.3			AIN3	CMP2		PWM03						INT03B
22	18	-	-	P0.2			AIN2	CMP1		PWM02						INT02B
23	19	15	-	P0.1			AIN1	CMP0	OP_P	PWM01						INT01B
24	20	16	-	P0.0			AIN0	CMPR	OP_N	PWM00						INT00B

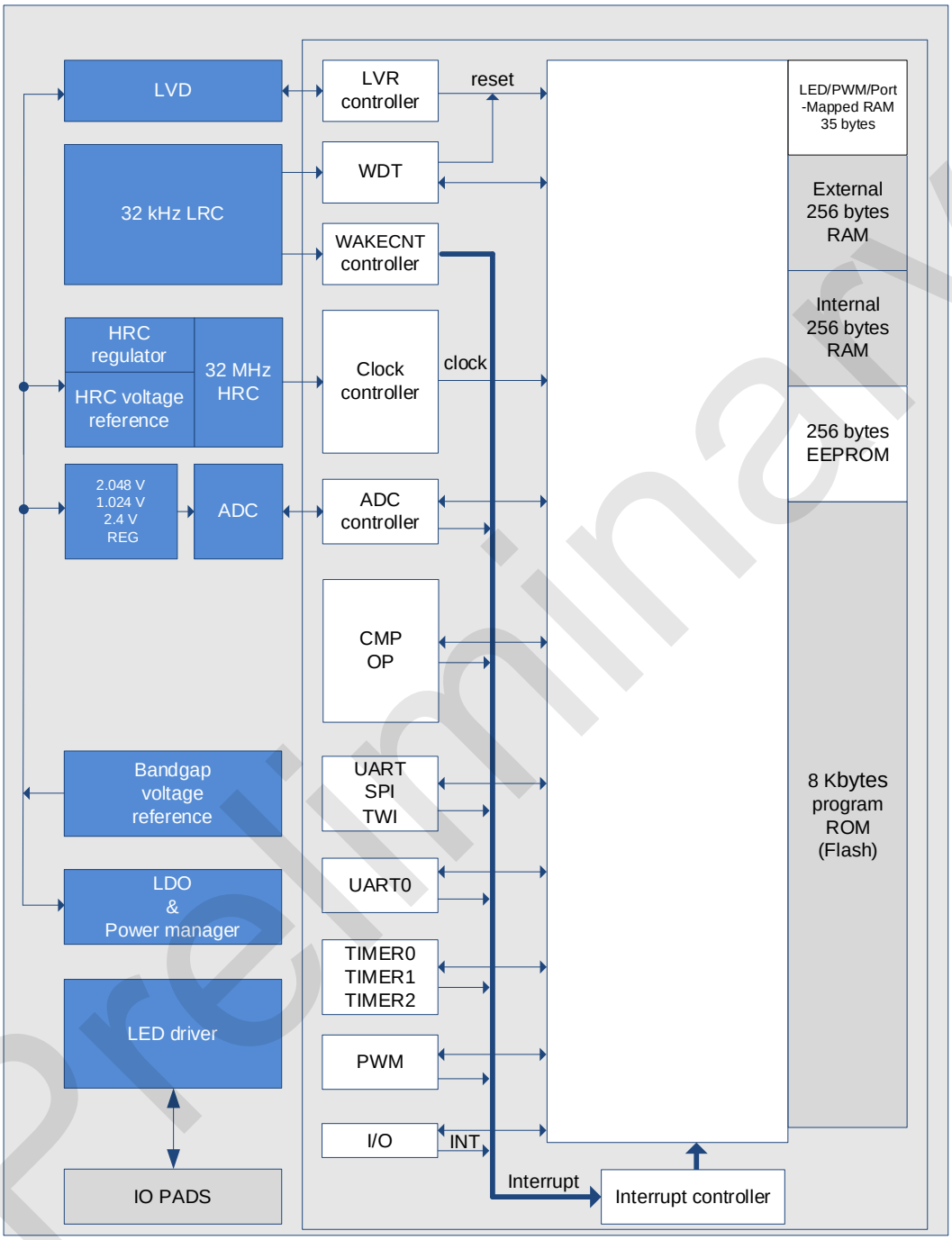
3.2.2 Pin Description

Pin Number				Pin Name	Pin Type	Function Description
24PIN	20PIN	16PIN	8PIN			
1	1	1	8	VDD	Power	Power supply
2	2	2	1	VSS	Power	Ground
3	3	3	-	P1.0/INT00A/AIN21	I/O	P1.0: GPIO P1.0 INT00A: External interrupt 0 input 0 multiplexed on group A AIN21: ADC input channel 21
4	4	4	-	P1.1/INT01A/AIN20/NRST	I/O	P1.1: GPIO P1.1 INT01A: External interrupt 0 input 1 multiplexed on group A AIN20: ADC input channel 20 NRST: External Reset pin
5	5	5	2	P1.2/INT02A/T0/RXD0/AIN19/tCK	I/O	P1.2: GPIO P1.2 INT02A: External interrupt 0 input 2 multiplexed on group A T0: Counter 0 external input RXD0: UART0 receive AIN19: ADC input channel 19 tCK: Programming and debugging port clock line
6	6	6	3	P1.3/INT03A/T1/TXD0/AIN18/tDIO	I/O	P1.3: GPIO P1.3 INT03A: Input 3 of External interrupt 0 mapped on Group A T1: External input of Counter 1 TXD0: UART0 Transmit AIN18: ADC input channel 18 tDIO: programming and debugging port data line
7	-	-	-	P1.4/INT04A/AIN17	I/O	P1.4: GPIO P1.4 INT04A: Input 4 of External interrupt 0 mapped on Group A AIN17: ADC input channel 17
8	-	-	-	P1.5/INT05A/AIN16	I/O	P1.5: GPIO P1.5 INT05A: Input 5 of External interrupt 0 mapped on Group A AIN16: ADC input channel 16
9	7	-	-	P2.7/INT15B/PWM07/AIN15/LED0	I/O	P2.7: GPIO P2.7 INT15B: External interrupt 1 input 5 multiplexed on group B PWM07: PWM07 output port AIN15: ADC input channel 15 LED0: LED bidirectional drive mode output port 0
10	8	7	4	P2.6/INT14B/PWM06/AIN14/LED1	I/O	P2.6: GPIO P2.6 INT14B: External interrupt 1 input 4 multiplexed on group B PWM06: PWM06 output port AIN14: ADC input channel 14 LED1: LED bidirectional drive mode output port 1

Pin Number				Pin Name	Pin Type	Function Description
24PIN	20PIN	16PIN	8PIN			
11	9	8	5	**P2.5/INT13B/PWM05/AIN13/LED2**	I/O	P2.5: GPIO P2.5 INT13B: External interrupt 1 input 3 multiplexed on group B PWM05: PWM05 output port AIN13: ADC input channel 13 LED2: LED bidirectional drive mode output port 2
12	10	9	-	**P2.4/INT12B/PWM04/AIN12/LED3**	I/O	P2.4: GPIO P2.4 INT12B: External interrupt 1 input 2 multiplexed on group B PWM04: PWM04 output AIN12: ADC input channel 12 LED3: LED bidirectional drive mode output 3
13	11	10	-	**P2.3/INT11B/AIN11/LED4**	I/O	P2.3: GPIO P2.3 INT11B: External interrupt 1 input 1 multiplexed on group B AIN11: ADC input channel 11 LED4: LED bidirectional drive mode output 4
14	12	11	-	**P2.2/INT10B/AIN10/LED5**	I/O	P2.2: GPIO P2.2 INT10B: External interrupt 1 input 0 multiplexed on group B AIN10: ADC input channel 10 LED5: LED bidirectional drive mode output 5
15	13	12	6	**P2.1/INT15A/MISO/RXD1/AIN9/LED6**	I/O	P2.1: GPIO P2.1 INT15A: Input 5 of External Interrupt 1 be multiplexed on Group A MISO: SPI Master Input Slave Output RXD1: UART1 Receive AIN9: ADC input channel 9 LED6: LED bidirectional drive mode output port 6
16	14	13	7	**P2.0/INT14A/MOSI/TXD1/SDA/AIN8/ LED7**	I/O	P2.0: GPIO P2.0 INT14A: Input 4 of External Interrupt 1 be multiplexed on Group A MOSI: SPI Master Output Slave Input TXD1: UART1 Transmit SDA: TWI SDA AIN8: ADC input channel 8 LED7: LED bidirectional drive mode output port 7
17	-	-	-	**P0.7/INT13A/T2/PWM20/AIN7**	I/O	P0.7: GPIO P0.7 INT13A: Input 3 of External interrupt 1 mapped on Group A T2: Counter 2 external input PWM20: PWM20 output AIN7: ADC input channel 7
18	-	-	-	**P0.6/INT12A/T2EX/PWM21/AIN6**	I/O	P0.6: GPIO P0.6 INT12A: Input 2 of External interrupt 1 mapped on Group A T2EX: Timer 2 external capture signal input

Pin Number				Pin Name	Pin Type	Function Description
24PIN	20PIN	16PIN	8PIN			
						PWM21: PWM21 output AIN6: ADC input channel 6
19	15	14	-	**P0.5/INT11A/INT05B/SCK/SCL/FLT/ AIN5/OP_O**	I/O	P0.5: GPIO P0.5 INT11A: Input 1 of External interrupt 1 mapped on Group A INT05B: Input 5 of External interrupt 0 mapped on Group B SCK: SCK of SPI SCL: SCL of TWI FLT: PWM0 fault detection input pin AIN5: ADC input channel 5 OP_O: OP output port
20	16	-	-	**P0.4/INT10A/INT04B/AIN4/CMP3**	I/O	P0.4: GPIO P0.4 INT10A: External interrupt 1 input 0 multiplexed on Group A INT04B: External interrupt 0 input 4 multiplexed on Group B AIN4: ADC input channel 4 CMP3: CMP positive input port 3
21	17	-	-	**P0.3/INT03B/PWM03/AIN3/CMP2**	I/O	P0.3: GPIO P0.3 INT03B: External interrupt 0 input 3 multiplexed on Group B PWM03: PWM03 output port AIN3: ADC input channel 3 CMP2: CMP positive input port 2
22	18	-	-	**P0.2/INT02B/PWM02/AIN2/CMP1**	I/O	P0.2: GPIO P0.2 INT02B: Input 2 of External interrupt 0 be multiplexed on group B PWM02: PWM02 output pin AIN2: ADC input channel 2 CMP1: CMP positive input pin 1
23	19	15	-	**P0.1/INT01B/PWM01/AIN1/CMP0 /OP_P**	I/O	P0.1: GPIO P0.1 INT01B: Input 1 of External interrupt 0 be multiplexed on group B PWM01: PWM01 output pin AIN1: ADC input channel 1 CMP0: CMP positive input pin 0 OP_P: OP non-inverting input terminal
24	20	16	-	**P0.0/INT00B/PWM00/AIN0/CMPR /OP_N**	I/O	P0.0: GPIO P0.0 INT00B: Input 0 of External interrupt 0 be multiplexed on group B PWM00: PWM00 output port AIN0: ADC input channel 0 CMPR: CMP negative external input port OP_N: OP inverting input terminal

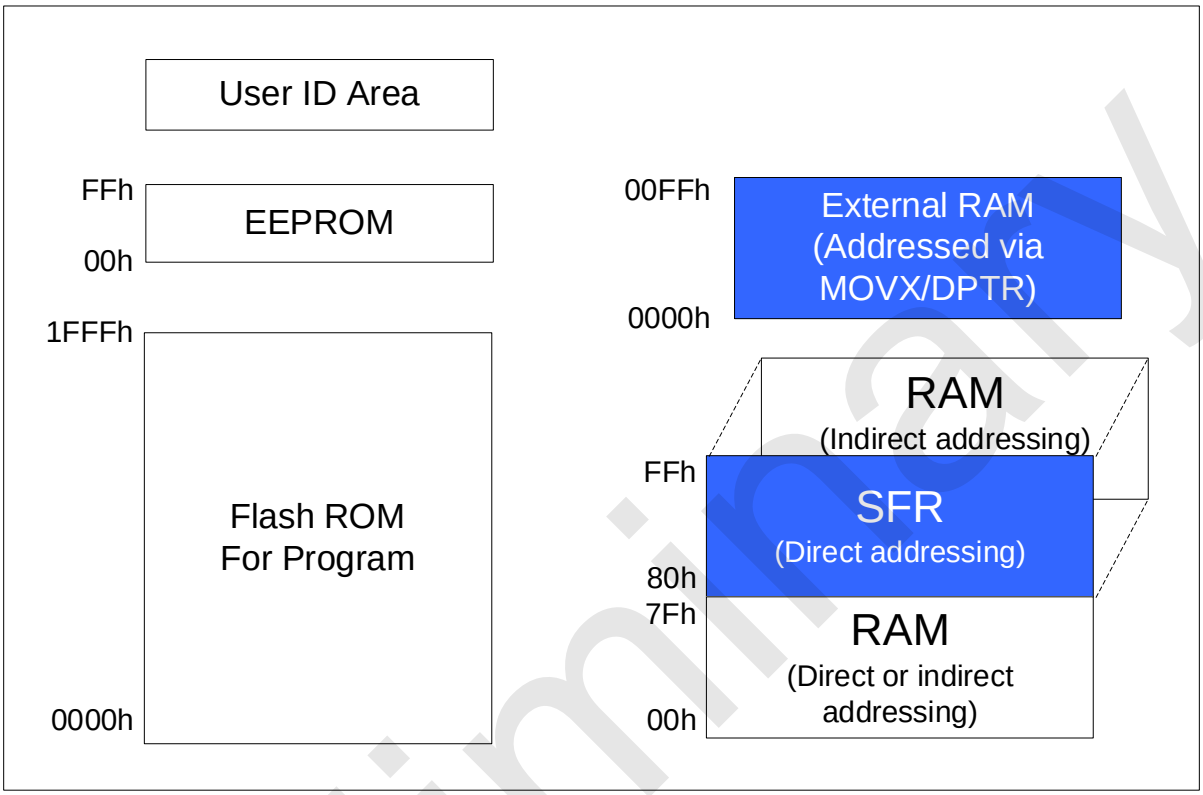
4 Internal block diagram



SC92F531X BLOCK DIAGRAM

5 ROM and SRAM structure

The ROM of SC92F531X is divided into four areas: 8 Kbytes Flash ROM / EEPROM / User ID / Unique ID, structured as shown below:



5.1 8 Kbytes Flash ROM

SC92F531X has 8 Kbytes of Flash ROM, with addresses ranging from 0000H to 1FFFH, programmable and erasable via the SinOne dedicated ICP programmer (SC LINK or SC LINK PRO). The features of this 8 Kbytes Flash ROM are as follows:

- Can be rewritten 1000 times
- Data retention of over 100 years at 25 ℃
- Supports blank checking (BLANK), programming (PROGRAM), verification (VERIFY), erasing (ERASE), and reading (READ) functions in ICP mode

Note: When programming the chip with a programmer, the programming voltage level must be set to 5V.

5.2 256 bytes independent EEPROM

The 256 bytes EEPROM is a segment separate from the 8 Kbytes Flash ROM, with addresses ranging from 00H to FFH. This section supports single-byte read and write operations during the program execution. For detailed instructions, refer to Read/write operations for EEPROM and Unique ID areas. Programming and erasing can be performed using the dedicated ICP programmer (SC LINK or SC LINK PRO) provided by SinOne.

The characteristics of this 256-byte EEPROM are as follows:

- The EEPROM supports 10,000 erase/write cycles. Users must not exceed the rated write cycles to prevent abnormalities

- Data retention of over 10 years at 25 ℃
- When performing write operations on the EEPROM, the V_{DD} must be maintained between 2.5 V and 5.5 V

5.3 Read/write operations for EEPROM and Unique ID areas

Users can read and write the 256-byte EEPROM area of the SC92F531X, and read the 96-bit Unique ID area.

5.3.1 Related registers for EEPROM operations

Description of related registers for EEPROM operations:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
IAPKEY	F1H	EEPROM Protection Register	IAPKEY[7:0]								00000000b
IAPAD	F2H	EEPROM Write Address Register	IAPADR[7:0]								00000000b
IAPADE	F4H	EEPROM Write Extended Address Register	IAPADER[7:0]								00000000b
IAPDAT	F5H	EEPROM Data Register	IAPDAT[7:0]								00000000b
IAPCTL	F6H	EEPROM Control Register	-	-	-	-	PAYTIMES[1:0]		CMD	EBUSY	xxxx0000b

IAPKEY (F1H) EEPROM Protection Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPKEY[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	IAPKEY[7:0]	Enable EEPROM R/W function and operation timeout settings Write a value n ≥ 0x40, indicating: Enable EEPROM R/W function If no write command is received within n system clock cycles, the EEPROM R/W function will be disabled.

IAPAD (F2H) EEPROM Write Address Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPADR[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	IAPADR[7:0]	EEPROM write address

IAPADE (F4H) EEPROM Write Extended Address Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPADER[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	IAPADER[7:0]	EEPROM write extended address: 0x01: Read-only operation for the Unique ID area; writing is prohibited. 0x02: Read/write operations for the EEPROM area Others: reserved

IAPDAT (F5H) EEPROM Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	IAPDAT[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	IAPDAT	Data Written to EEPROM

IAPCTL(F6H) EEPROM Control Register

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	PAYTIMES[1:0]		CMD	EBUSY
Read/Write	-	-	-	-	R/W	R/W	W	R
Power-On Initial Value	x	x	x	x	0	0	0	0

Bit Number	Bit Symbol	Description
3-2	**PAYTIMES[1:0]**	EEPROM write duration setting 00: Set write time to 4 ms @ V_{DD}=5V 01: Set write time to 2 ms @ V_{DD}=5V 10: Set write time to 1 ms @ V_{DD}=5V 11: Reserved Note: CPU can operate normally during EEPROM write operations
1	CMD	EEPROM command enable bit (write-only, not readable) 1: Execute write or erase command 0: No operation
0	EBUSY	EEPROM read/write wait status bit (read-only) 0: EEPROM operation idle or completed 1: EEPROM operation in progress

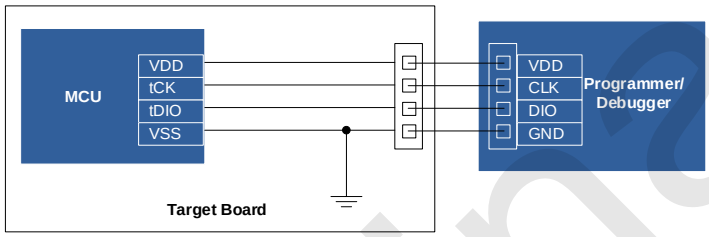
Bit Number	Bit Symbol	Description
7-4	-	Reserved

5.3.2 EEPROM operation procedure

For SC92F531X EEPROM operation procedure and precautions, please refer to the 'SC92F531X IAP Operation Library Package'.

5.4 Programming

The Flash ROM and EEPROM of the SC92F531X can be programmed via tDIO, tCK, VDD, and VSS. The specific connection details are as follows:



ICP mode programming connection diagram

tDIO and tCK are signal lines for 2-wire JTAG programming and debugging. Users can configure the mode of these two ports through the Customer Option item during programming:

5.4.1 JTAG dedicated mode

tDIO and tCK serve as dedicated ports for programming and debugging, and other multiplexed functions are disabled. This mode is typically used for online debugging Once the JTAG dedicated mode is enabled, the chip can enter programming or debugging mode directly without power cycling.

5.4.2 Normal mode (JTAG dedicated port disabled)

The JTAG function is unavailable, other multiplexed functions can be used normally. This mode prevents the programming port from occupying MCU pins, allowing users to maximize MCU resources.

Note: After successfully configuring the JTAG dedicated port as disabled, the chip must be fully powered off and then powered back on to enter programming or debugging mode. This will affect programming and debugging in power-on mode. SinOne recommends users select the JTAG dedicated port disabled configuration for mass production programming and select JTAG mode during the R&D and debugging phase.

Related customer option registers are as follows:

OP_CTM1 (C2H@FFH) Code Option register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	VREFS[1:0]		-	DISJTG	-	-	-	-
Read/Write	R/W	R/W	-	R/W	-	-	-	-
Power-On Initial Value	n	n	x	n	x	x	x	x

Bit Number	Bit Symbol	Description
4	DISJTG	IO/JTAG port switching control

Bit Number	Bit Symbol	Description
		0: JTAG mode enabled, P1.2 and P1.3 can only be used as tCK and tDIO. Recommended setting during R&D debugging phase. 1: Normal mode, JTAG function disabled. Recommended setting during mass production programming phase.

5.5 Customer Option area (user programming setting)

The SC92F531X contains a separate internal Flash area to store user power-on initial value settings, called the Code Option area. When programming the IC, users write this part of the code into the IC. During reset initialization, the IC loads these settings into the SFR as the initial values.

Option-related SFR operation instructions:

The read and write operations of Option-related SFRs are controlled by the OPINX and OPREG registers. The specific location of each Option SFR is determined by OPINX, as shown in the table below:

Symbol	Address	Description	7	6	5	4	3	2	1	0
OP_CTM0	C1H@FFH	Customer Option register 0	ENWDT	DRV_EH	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
OP_CTM1	C2H@FFH	Customer Option register 1	VREFS[1:0]		-	DISJTG	-	-		
OP_HRCR	83H@FFH	System clock change register	-	-	OP_HRCR[5:0]					

IFB Address	Symbol	R/W	Description
OP_CTM0[7]	ENWDT	R/W	**WDT enable switch** 0: WDT disabled 1: WDT enabled
OP_CTM0[6]	DRV_EH	R/W	**LED port sourcing current I_{OL} drive capability selection:** 0: For ports corresponding to LED0 through LED7, only those enabled for LED function have strong drive capability of sourcing current I_{OL} ports not enabled retain regular drive capability. For non-LED driving applications, it is recommended to use the regular drive capability of these ports. 1: The ports corresponding to LED0 through LED7 have a sourcing current I_{OL} with always strong driving capability.
OP_CTM0[5-4]	SCLKS[1:0]	R/W	**System clock frequency (f_{SYS}) selection:** 00: System clock frequency equals High-Frequency Oscillator frequency divided by 1 01: System clock frequency equals High-Frequency Oscillator frequency divided by 2 10: System clock frequency equals High-Frequency Oscillator frequency divided by 4 11: System clock frequency equals High-Frequency Oscillator frequency divided by 12.
OP_CTM0[3]	DISRST	R	**IO/RST switching control** 0: P1.1 used as Reset pin (NRST) 1: P1.1 used as normal I/O pin
OP_CTM0[2]	DISLVR	R/W	**LVR switch** 0: LVR enabled 1: LVR disabled
OP_CTM0[1-0]	LVRS [1:0]	R/W	**LVR Voltage Selection Control** 11: 4.3V Reset 10: 3.7V Reset

<table>
<tr><th>IFB Address</th><th>Symbol</th><th>R/W</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>01: 2.9V Reset
00: 2.3V Reset</td></tr>
<tr><td>OP_CTM1[7-6]</td><td>VREFS[1:0]</td><td>R/W</td><td>Reference Voltage Selection (initial value loaded from Code Option, user can modify settings)
00: Set ADC VREF to V_{DD}
01: Set ADC VREF to internal accurate 1.024V
10: Set ADC VREF to internal accurate 2.4V
11: Set ADC VREF to internal accurate 2.048V.</td></tr>
<tr><td>OP_CTM1[4]</td><td>DISJTG</td><td>R/W</td><td>IO/JTAG port switching control
0: JTAG mode enabled, P1.2 and P1.3 can only be used as tCK and tDIO signals
1: Normal Mode, JTAG function ineffective</td></tr>
<tr><td>OP_HRCR</td><td>OP_HRCR[5:0]</td><td>R/W</td><td>HRC frequency adjustment register
The center value (10000000b) corresponds to the HRC center frequency. Increasing this value raises the frequency, while decreasing it lowers the frequency.
Users can modify the value of this register to change the high-frequency oscillator frequency f_{HRC}, thereby adjusting the IC's system clock frequency f_{SYS}:
1. The initial power-on value OP_HRCR[5:0], denoted OP_HRCR[s], is fixed to ensure f_{HRC} is 32 MHz, though the OP_HRCR[s] value may vary between individual ICs
2. With the initial value set to OP_HRCR[s], the IC's system clock frequency f_{SYS} can be accurately configured to 32, 16, 8, or 2.66 MHz via the Option item. Each increment of 1 in OP_HRCR[5:0] changes the f_{SYS} frequency by approximately 0.5%.
The relationship between OP_HRCR [5:0] and f_{SYS} output frequency is as follows:
<table>
<tr><td>OP_HRCR [5:0] value</td><td>f_{SYS} actual output frequency (using 32 MHz as an example)</td></tr>
<tr><td>OP_HRCR [s]-n</td><td>32000*(1-0.5%*n)kHz</td></tr>
<tr><td>...</td><td>....</td></tr>
<tr><td>OP_HRCR [s]-2</td><td>32000*(1-0.5%*2)= 31680 kHz</td></tr>
<tr><td>OP_HRCR [s]-1</td><td>32000*(1-0.5%*1)= 31840 kHz</td></tr>
<tr><td>OP_HRCR [s]</td><td>32000 kHz</td></tr>
<tr><td>OP_HRCR [s]+1</td><td>32000*(1+0.5%*1)= 32160 kHz</td></tr>
<tr><td>OP_HRCR [s]+2</td><td>32000*(1+0.5%*2)= 32320 kHz</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>OP_HRCR [s]+n</td><td>32000*(1+0.5%*n)kHz</td></tr>
</table>
Note:
1. After each power-on, the IC sets OP_HRCR [5:0] to the High-Frequency Oscillator frequency f_{HRC} closest to 32 MHz
2. To ensure reliable IC operation, the maximum operating frequency should preferably not exceed 10% above 32 MHz, i.e., 35.2 MHz
3. Ensure that changing the HRC frequency will not affect other functions.</td></tr>
</table>

5.5.1 Option related SFR operation description

Read and write operations of Option-related SFRs are controlled by the OPINX and OPREG registers. OPINX specifies the address of the Option SFR, while OPREG holds the value to be written:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
OPINX	FEH	Option Pointer	OPINX[7:0]								00000000b
OPREG	FFH	Option Register	OPREG[7:0]								nnnnnnnnb

When operating Option-related SFRs, OPINX stores the address of the target OPTION register, and OPREG stores the corresponding data.

For example, to configure OP_HRCR to 0x01, proceed as follows:

C language example:

OPINX = 0x83 // Write the address of OP_HRCR into the OPINX register

OPREG = 0x01 // Write 0x01 into the OPREG register (value to be written to OP_HRCR)

Assembly routine:

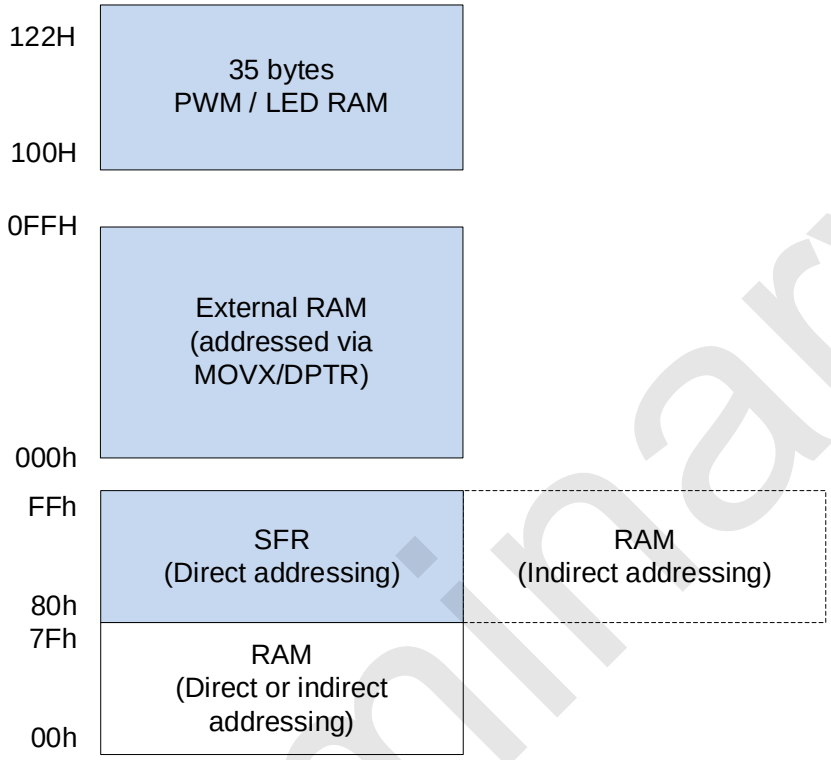
MOV OPINX,#83H Write the address of OP_HRCR to the OPINX register

MOV OPREG,#01H Write 0x01 to the OPREG register (the value to be written to the OP_HRCR register

Note: It is prohibited to write any value outside the SFR addresses of the Customer Option area to the OPINX register. Otherwise, system malfunctions may occur.

5.6 SRAM

The SRAM structure of the SC92F531X is as follows:



The SC92F531X microcontroller integrates 0.5Kbytes of SRAM internally, divided into 256 bytes of internal RAM and 256 bytes of external RAM. The address range of the internal RAM is from 00H to FFH, where the upper 128 bytes (addresses 80H to FFH) are only accessible via indirect addressing, and the lower 128 bytes (addresses 00H to 7FH) can be accessed through both direct and indirect addressing.

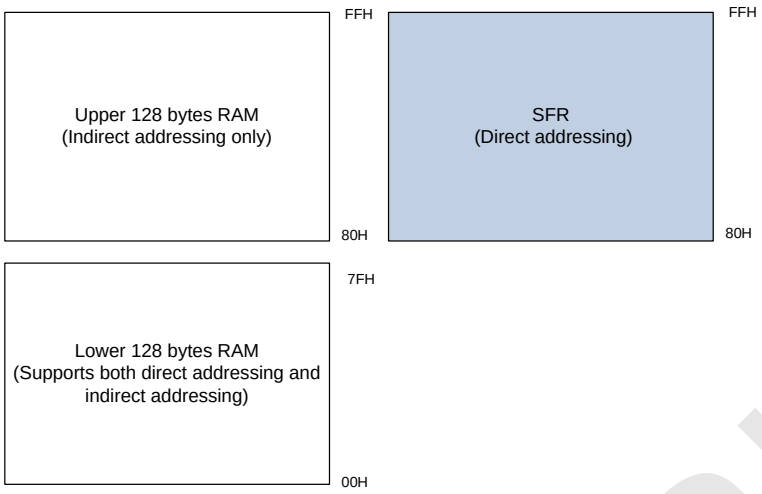
The Special Function Registers (SFR) are also located in the address range from 80H to FFH. But the difference lies in that SFR registers use direct addressing, whereas the internal upper 128 bytes SRAM can only be accessed via indirect addressing.

The address range of external RAM is 00H-FFH, but it must be accessed using the MOVX instruction.

35 bytes PWM / LED RAM, see details below 35 Bytes register extended RAM.

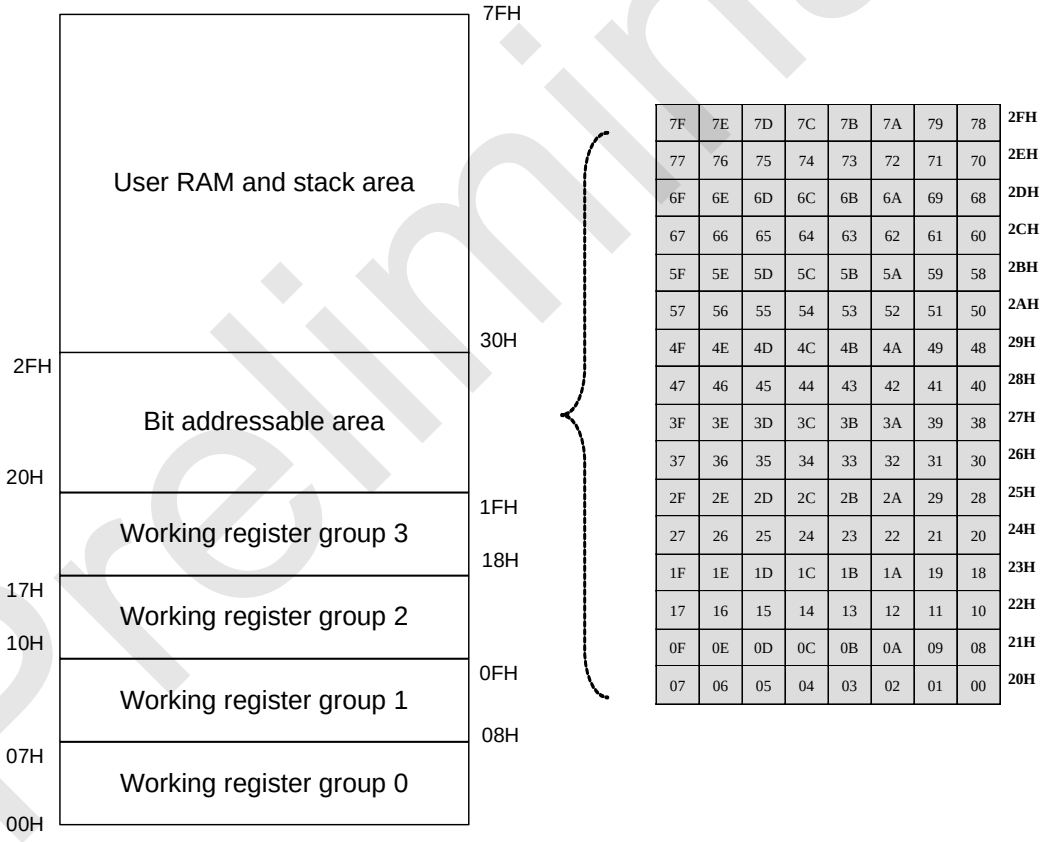
5.6.1 Internal 256 bytes SRAM

The internal lower 128 bytes SRAM area can be divided into three parts: ① Working register groups 0-3, with addresses from 00H to 1FH the RS0 and RS1 bits in the program status word PSW determine the currently used working register group, which can accelerate computation ② Bit Addressing area from 20H to 2FH, which can be used either as general RAM or as bit-addressable RAM In Bit Addressing, the bit Address ranges from 00H to 7FH (this address is bit-addressed, unlike general SRAM which is byte-addressed), and can be distinguished by Instructions in the program ③ User RAM and Stack region: after SC92F531X Reset, the 8-bit Stack Pointer points to the Stack region. Users typically set the initial value during initialization, and it is recommended to set it within the address range E0H-FFH.



Internal 256 bytes RAM structure diagram

The internal lower 128 bytes RAM structure is as follows:



SRAM structure diagram

5.6.2 External 256 bytes SRAM

External 256-byte RAM can be accessed via MOVX @DPTR, A It is also possible to access external 256-byte RAM using MOVX A, @Ri or MOVX @Ri, A.

6 Special Function Register (SFR)

6.1 SFR mapping

The SC92F531X series has a set of special function registers, referred to as SFR. The addresses of these SFR registers range from 80H to FFH. Some support bit addressing, while others do not. Registers supportting bit addressing have addresses ending with "0" or "8", which makes it convenient to modify individual bits. All SFRs must be accessed using direct addressing.

The names and addresses of the SC92F531X special function registers are listed in the following table:

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8h	-	-	-	-	CHKSUML	CHKSUMH	OPINX	OPREG
F0h	B	IAPKEY	IAPAD	-	IAPADE	IAPDAT	IAPCTL	-
E8h	-	EXA0	EXA1	EXA2	EXA3	EXBL	EXBH	OPERCON
E0h	ACC	-	-	-	-	-	-	-
D8h	-	-	-	-	-	-	-	-
D0h	PSW	PWMCFG	PWMCON0	PWMCON1	PWMPDL	PWMPDH	PWMDFR	PWMFLT
C8h	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	BTMCON	WDTCON
C0h	-	-	-	-	-	-	-	-
B8h	IP	IP1	INT0F	INT0R	INT1F	INT1R	-	-
B0h	-	-	-	-	ZOCINX	-	ZOCCFG	ZOCCON
A8h	IE	IE1	ADCCFG2	ADCCFG0	-	ADCCON	ADCVL	ADCVH
A0h	P2	P2CON	P2PH	-	COMCON	-	DDRCON2	-
98h	SCON	SBUF	P0CON	P0PH	LEDVO0	SSCON0	SSCON1	SSDAT
90h	P1	P1CON	P1PH	-	-	SSCON2	DDRCON0	SCANCON
88h	TCON	TMOD	TL0	TL1	TH0	TH1	TMCON	OTCON
80h	P0	SP	DPL	DPH	-	-	-	PCON
	Bit addressing available	Bit addressing not available						

Note:

1. **Empty cells in the SFR register indicate reserved addresses. For those registers users are not recommended to use them.**
2. **F1H-FFH in the SFR are Special Function Registers reserved for system configuration. User's modification may cause system errors. Users should not clear or otherwise operate on these registers during system initialization.**

6.2 SFR Description

The detailed explanation of the Special Function Registers (SFR) is as follows:

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
P0	80H	P0 Port Data Register	P07	P06	P05	P04	P03	P02	P01	P00	00000000b
SP	81H	Stack Pointer	SP[7:0]								00000111b
DPL	82H	DPTR Data Pointer Low Byte	DPL[7:0]								00000000b
DPH	83H	DPTR Data Pointer High Byte	DPH[7:0]								00000000b
PCON	87H	Power Supply Management Control Register	SMOD	-	-	-	RST	-	STOP	IDL	0xxx0x00b

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
TCON	88H	Timer Control Register	TF1	TR1	TF0	TR0	IE1	-	IE0	-	00000x0xb
TMOD	89H	Timer Operating Mode Register	-	C/T1	M11	M01	-	C/T0	M10	M00	x000x000b
TL0	8AH	Timer 0 Low Byte	TL0[7:0]								00000000b
TL1	8BH	Timer 1 Low Byte	TL1[7:0]								00000000b
TH0	8CH	Timer 0 High Byte	TH0[7:0]								00000000b
TH1	8DH	Timer 1 High Byte	TH1[7:0]								00000000b
TMCON	8EH	Timer Frequency Control Register	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b
OTCON	8FH	Output Control Register	SSMOD[1:0]		-	-	-	-	-	-	00xxxxxb
P1	90H	P1 Port Data Register	-	-	P15	P14	P13	P12	P11	P10	xx000000b
P1CON	91H	P1 Port Input/Output Control Register	-	-	P1C5	P1C4	P1C3	P1C2	P1C1	P1C0	xx000000b
P1PH	92H	P1 Port Pull-up Resistor Control Register	-	-	P1H5	P1H4	P1H3	P1H2	P1H1	P1H0	xx000000b
SSCON2	95H	SSI Control Register 2	SSCON2[7:0]								00000000b
DDRCON0	96H	Display Driver Control Register	DDRON	-	-		-		-		0xxxxxxb
SCANCON	97H	Display Driver Scan Configuration Register	AUIF	CMEN	LEDXT[1:0]		LTSEL[1:0]		DISPCK [1:0]		00010000b
SCON	98H	Serial Port Control Register	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00000000b
SBUF	99H	Serial Port Data Buffer Register	SBUF[7:0]								00000000b
P0CON	9AH	P0 Port Input/Output Control Register	P0C7	P0C6	P0C5	P0C4	P0C3	P0C2	P0C1	P0C0	00000000b
P0PH	9BH	P0 Port Pull-up Resistor Control Register	P0H7	P0H6	P0H5	P0H4	P0H3	P0H2	P0H1	P0H0	00000000b
LEDVO0	9CH	LED Display Driver Output Register 0	LED7VO	LED6VO	LED5VO	LED4VO	LED3VO	LED2VO	LED1VO	LED0VO	00000000b
SSCON0	9DH	SSI Control Register 0	SSCON0[7:0]								00000000b
SSCON1	9EH	SSI Control Register 1	SSCON1[7:0]								00000000b
SSDAT	9FH	SSI Data Register	SSD[7:0]								00000000b
P2	A0H	P2 Port Data Register	P27	P26	P25	P24	P23	P22	P21	P20	00000000b
P2CON	A1H	P2 Port Input/Output Control Register	P2C7	P2C6	P2C5	P2C4	P2C3	P2C2	P2C1	P2C0	00000000b
P2PH	A2H	P2 Port Pull-up Resistor Control Register	P2H7	P2H6	P2H5	P2H4	P2H3	P2H2	P2H1	P2H0	00000000b
COMCON	A4H	COM Port Control Register	COMFB7	COMFB6	COMFB5	COMFB4	COMFB3	COMFB2	COMFB1	COMFB0	00000000b
DDRCON2	A6H	Display Driver Control Register 2	-	-	-	-	DRIV[3:0]				xxxx1111b
IE	A8H	Interrupt Enable Register	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0	00000000b
IE1	A9H	Interrupt Enable Register 1	-	-	ECMP	-	-	EBTM	EPWM	ESSI	xx0xx000b
ADCCFG2	AAH	ADC Configuration Register 2	AINX[1:0]		-	LOWSP[2:0]			-	-	00x000xxb
ADCCFG0	ABH	ADC Configuration Register 0	EAINx[7:0]								00000000b

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
ADCCON	ADH	ADC Control Register	ADCEN	ADCS	ADCIF	ADCIS[4:0]					00000000b
ADCVL	AEH	ADC Result Register	ADCV[3:0]				-	-	-	-	1111xxxxb
ADCVH	AFH	ADC Result Register	ADCV[11:4]								11111111b
ZOCINX	B4H	ZOC Index Register	ZOCMOD[1:0]		-	-	-	-	-	-	00xxxxxxb
ZOCCFG	B6H	ZOC Setup Register	ZOCCFG[7:0]								00000000b
ZOCCON	B7H	ZOC Control Register	ZOCCON[7:0]								00000000b
IP	B8H	Interrupt Priority Control Register	-	IPADC	IPT2	IPUART0	IPT1	IPINT1	IPT0	IPINT0	x0000000b
IP1	B9H	Interrupt Priority Control Register 1	-	-	IPCMP	-	-	IPBTM	IPPWM	IPSSI	xx0xx000b
INT0F	BAH	INT0 Falling Edge Interrupt Control Register	-	-	INT0F5	INT0F4	INT0F3	INT0F2	INT0F1	INT0F0	xx000000b
INT0R	BBH	INT0 Rising Edge Interrupt Control Register	-	-	INT0R5	INT0R4	INT0R3	INT0R2	INT0R1	INT0R0	xx000000b
INT1F	BCH	INT1 Falling Edge Interrupt Control Register	-	-	INT1F5	INT1F4	INT1F3	INT1F2	INT1F1	INT1F0	xx000000b
INT1R	BDH	INT1 Rising Edge Interrupt Control Register	-	-	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0	xx000000b
T2CON	C8H	Timer 2 Control Register	TF2	E2F2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000b
T2MOD	C9H	Timer 2 working mode register	T2FD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN	0x000000b
RCAP2L	CAH	Timer 2 Reload Low 8 Bits	RCAP2L[7:0]								00000000b
RCAP2H	CBH	Timer 2 Reload High 8 Bits	RCAP2H[7:0]								00000000b
TL2	CCH	Timer 2 Low 8 Bits	TL2[7:0]								00000000b
TH2	CDH	Timer 2 High 8 Bits	TH2[7:0]								00000000b
BTMCON	CEH	Low-Frequency Timer Control Register	ENBTM	BTMIF	-	-	BTMFS[3:0]				00xx0000b
WDTCON	CFH	WDT Control Register	-	-	-	CLRWDT	-	WDTCKS[2:0]			xxx0x000b
PSW	D0H	Program Status Word Register	CY	AC	F0	RS1	RS0	OV	F1	P	00000000b
PWMCFG	D1H	PWM Setting Register	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0	00000000b
PWMCON0	D2H	PWM Control Register 0	ENPWM	PWMIF	PWMCK[1:0]		-	-	PWMMD[1:0]		0000xx00b
PWMCON1	D3H	PWM Control Register 1	ENPWM7	ENPWM6	ENPWM5	ENPWM4	ENPWM3	ENPWM2	ENPWM1	ENPWM0	00000000b
PWMPDL	D4H	PWM Period Register Low 8 bits	PWMPDL[7:0]								00000000b
PWMPDH	D5H	PWM Period Register High 8 bits	PWMPDH[7:0]								00000000b
PWMDFR	D6H	PWM Dead Time Setting Register	PDF[3:0]				PDR[3:0]				00000000b
PWMFLT	D7H	PWM Fault Detection Setting Register	FLTEN1	FLTSTA1	FLTMD1	FLTLV1	-	-	FLTDT1[1:0]		0000xx00b
ACC	E0H	Accumulator	ACC[7:0]								00000000b
EXA0	E9H	Extended Accumulator 0	EXA[7:0]								00000000b

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
EXA1	EAH	Extended Accumulator 1	EXA[15:8]								00000000b
EXA2	EBH	Extended Accumulator 2	EXA[23:16]								00000000b
EXA3	ECH	Extended Accumulator 3	EXA[31:24]								00000000b
EXBL	EDH	Extended Register B Low	EXB [7:0]								00000000b
EXBH	EEH	Extended Register B High	EXB [15:8]								00000000b
OPERCON	EFH	Operation Control Register	OPERS	MD	-	-	-	-	-	CHKSUMS	00xxxxx0b
B	F0H	Register B	B[7:0]								00000000b
IAPKEY	F1H	EEPROM Protection Register	IAPKEY[7:0]								00000000b
IAPAD	F2H	EEPROM Write Address Register	IAPADR[7:0]								00000000b
IAPADE	F4H	EEPROM Write Extended Address Register	IAPADER[7:0]								00000000b
IAPDAT	F5H	EEPROM Data Register	IAPDAT[7:0]								00000000b
IAPCTL	F6H	EEPROM Control Register	-	-	-	-	PAYTIMES[1:0]		CMD	EBUSY	xxxx0000b
CHKSUML	FCH	Checksum Result Register Low Byte	CHKSUML[7:0]								00000000b
CHKSUMH	FDH	Checksum Result Register High Byte	CHKSUMH[7:0]								00000000b
OPINX	FEH	Option Pointer	OPINX[7:0]								00000000b
OPREG	FFH	Option Register	OPREG[7:0]								nnnnnnnnb

6.2.1 35 Bytes register extended ram

RAM Partition	Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LED RAM 8 bytes	100H	LED0-	7	6	5	4	3	2	1	-
	101H	LED1-	15	14	13	12	11	10	-	0
	102H	LED2-	23	22	21	20	19	-	9	8
	103H	LED3-	31	30	29	28	-	18	17	16
	104H	LED4-	39	38	37	-	27	26	25	24
	105H	LED5-	47	46	-	36	35	34	33	32
	106H	LED6-	55	-	45	44	43	42	41	40
	107H	LED7-	-	54	53	52	51	50	49	48
PWM00-PWM07 Duty 16 bytes	108H	PWM0 DUTY PWM00-07	PDT00[15:8]							
	109H		PDT00[7:0]							
	10AH		PDT01[15:8]							
	10BH		PDT01[7:0]							
	10CH		PDT02[15:8]							
	10DH		PDT02[7:0]							
	10EH		PDT03[15:8]							
	10FH		PDT03[7:0]							
	110H		PDT04[15:8]							
	111H		PDT04[7:0]							

RAM Partition	Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
	112H		PDT05[15:8]							
	113H		PDT05[7:0]							
	114H		PDT06[15:8]							
	115H		PDT06[7:0]							
	116H		PDT07[15:8]							
	117H		PDT07[7:0]							
PWM20-PWM21 Duty 4 bytes	118H	PWM2 DUTY	PDT20[15:8]							
	119H		PDT20[7:0]							
	11AH		PDT21[15:8]							
	11BH		PDT21[7:0]							
PORT Mapped Register 7 bytes	11CH	SPOS_PWM21	-	-	-	PWM21SCL[4:0]				
	11DH	SPOS_SSICK	-	-	-	SSICKSEL[4:0]				
	11EH	SPOS_SSITX	-	-	-	SSITXSEL[4:0]				
	11FH	SPOS_SSIRX	-	-	-	SSIRXSEL[4:0]				
	120H	SPOS_TX0	-	-	-	TX0SEL[4:0]				
	121H	SPOS_RX0	INTSEL	-	-	RX0SEL[4:0]				
	122H	SPOS_T2EX	-	-	-	T2EXSEL[4:0]				

6.2.1.1 Bidirectional DriveMode LED Display RAM

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
100H	LED0-	7	6	5	4	3	2	1	-
101H	LED1-	15	14	13	12	11	10	-	0
102H	LED2-	23	22	21	20	19	-	9	8
103H	LED3-	31	30	29	28	-	18	17	16
104H	LED4-	39	38	37	-	27	26	25	24
105H	LED5-	47	46	-	36	35	34	33	32
106H	LED6-	55	-	45	44	43	42	41	40
107H	LED7-	-	54	53	52	51	50	49	48

6.2.1.2 PWM0 Duty Cycle Adjustment Register (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
108H	PDT00[15:8]								00000000b
109H	PDT00[7:0]								00000000b
10AH	PDT01[15:8]								00000000b
10BH	PDT01[7:0]								00000000b
10CH	PDT02[15:8]								00000000b
10DH	PDT02[7:0]								00000000b
10EH	PDT03[15:8]								00000000b
10FH	PDT03[7:0]								00000000b
110H	PDT04[15:8]								00000000b
111H	PDT04[7:0]								00000000b
112H	PDT05[15:8]								00000000b
113H	PDT05[7:0]								00000000b
114H	PDT06[15:8]								00000000b

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
115H	PDT06[7:0]								00000000b
116H	PDT07[15:8]								00000000b
117H	PDT07[7:0]								00000000b

6.2.1.3 PWM2 Duty Cycle Adjustment Register (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
118H	PDT20[15:8]								00000000b
119H	PDT20[7:0]								00000000b
11AH	PDT21[15:8]								00000000b
11BH	PDT21[7:0]								00000000b

6.2.1.4 Port mapped register (R/ W)

SSICK0, SSITX0, SSIRX0, TXD0, RXD0, and PWM21 ports of SC92F531X support full pin multiplexing users can configure the mapped port locations through the following Registers:

Symbol	Address	Function	7	6	5	4	3	2	1	0	Initial value
SPOS_PWM21	11CH	PWM21 mapped Register	-	-	-	PWM21SCL[4:0]					xxx00110b
SPOS_SSICK	11DH	SSI CLK mapped Register	-	-	-	SSICKSEL[4:0]					xxx00101b
SPOS_SSITX	11EH	SSI TX mapped Register	-	-	-	SSITXSEL[4:0]					xxx01000b
SPOS_SSIRX	11FH	SSI RX mapped Register	-	-	-	SSIRXSEL[4:0]					xxx01001b
SPOS_TX0	120H	UART0 TX mapped Register	-	-	-	TX0SEL[4:0]					xxx10100b
SPOS_RX0	121H	UART0 RX mapped Register	INTSEL	-	-	RX0SEL[4:0]					0xx10101b
SPOS_T2EX	122H	T2EX mapped Register				T2EXSEL[4:0]					xxx00110b

6.2.1.5 Signal multiplexing settings

The pin multiplexing ports (SSICK0, SSITX0, SSIRX0) support the following functions. These ports are configured via the three-in-one serial port module:

- Selecting SPI function: SSICK0 corresponds to SCK, SSITX0 corresponds to MOSI, and SSIRX0 corresponds to MISO
- Selecting TWI function: SSICK0 corresponds to SCL, and SSITX0 corresponds to SDA
- Selecting UART function: SSITX0 corresponds to TXD1, and SSIRX0 corresponds to RXD1

To configure multiplexed pins, write the appropriate values to the corresponding multiplexing registers. To multiplex the PWM21 port onto pin P0.1, first define a variable corresponding to the address of the PWM21 multiplexing register in RAM, such as SPOS_PWM21, then write the value 0x01 to the SPOS_PWM21 variable to achieve the multiplexing. The specific pins that are multiplexed and their corresponding configuration values are shown in the following table, which includes the default multiplexed pin information for each port:

Serial Number	Configuration Value	Pin Multiplexing	Default Port - Communication	Default Port - PWM21	Default Port - T2EX	INTSEL = 0	INTSEL = 1
0	00000	P0.0	-	-	-	-	INT00
1	00001	P0.1	-	-	-	-	INT01

Serial Number	Configuration Value	Pin Multiplexing	Default Port - Communication	Default Port - PWM21	Default Port - T2EX	INTSEL = 0	INTSEL = 1
2	00010	P0.2	-	-	-	-	INT02
3	00011	P0.3	-	-	-	-	INT03
4	00100	P0.4	-	-	-	INT10	INT04
5	00101	P0.5	SSICK0	-	-	INT11	INT05
6	00110	P0.6	-	PWM21	T2EX	INT12	-
7	00111	P0.7	-	-	-	INT13	-
8	01000	P2.0	SSITX0	-	-	INT14	-
9	01001	P2.1	SSIRX0	-	-	INT15	-
10	01010	P2.2	-	-	-	-	INT10
11	01011	P2.3	-	-	-	-	INT11
12	01100	P2.4	-	-	-	-	INT12
13	01101	P2.5	-	-	-	-	INT13
14	01110	P2.6	-	-	-	-	INT14
15	01111	P2.7	-	-	-	-	INT15
18	10010	P1.5	-	-	-	INT05	-
19	10011	P1.4	-	-	-	INT04	-
20	10100	P1.3	TXD0	-	-	INT03	-
21	10101	P1.2	RXD0	-	-	INT02	-
22	10110	P1.1	-	-	-	INT01	-
25	11001	P1.0	-	-	-	INT00	-
X	Others	Reserved	-	-	-		-

The definition of the external interrupt port multiplexing bits is as follows:

Bit Number	Bit Symbol	Description
7	**INTSEL**	Multiplexing selection bits for the external interrupt port 0: Select Group A multiplexing 1: Select Group B multiplexing

6.2.2 Introduction to Commonly Used Special Function Registers of the 8051 CPU Core

6.2.2.1 Program Counter PC

The program counter PC is not part of the SFR register set. The PC is 16-bit and is used to control the sequence of instruction execution. After microcontroller power-on or reset, the PC value is 0000H, which means the microcontroller program starts executing from address 0000H.

6.2.2.2 Accumulator ACC (E0H)

The Accumulator ACC is one of the most frequently used registers in the 8051 core microcontroller. The instruction set uses A as its mnemonic. It typically stores operands and results for arithmetic and logical operations.

6.2.2.3 Register B (F0H)

Register B must be used together with Accumulator A during multiplication and division operations. The multiplication instruction MUL A, B multiplies the 8-bit unsigned values in Accumulator A and Register B. The 16-bit product's low byte is stored in A, while the high byte is stored in B. The division instruction DIV A, B divides A by B, storing the integer quotient in A and the remainder in B. Register B can also serve as a general-purpose temporary register.

6.2.2.4 Stack Pointer SP (81H)

The Stack Pointer is an 8-bit special register that indicates the position of the top of the stack in general-purpose RAM. After microcontroller reset, the initial value of SP is 07H, so the stack starts growing upward from 08H. Addresses 08H to 1FH correspond to working register groups 1 to 3.

6.2.2.5 PSW (D0H) Program Status Word Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	CY	AC	F0	RS1	RS0	OV	F1	P
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**CY**	Flag Bit 1: When the highest bit of addition has a carry, or the highest bit of subtraction has a borrow 0: When the highest bit of addition has no carry, or the highest bit of subtraction has no borrow
6	**AC**	Auxiliary Carry Flag (used for convenient adjustment during BCD addition and subtraction) 1: Carry at bit 3 during addition or borrow at bit 3 during subtraction 0: No borrow or carry
5	**F0**	User flag bit
4-3	**RS1、RS0**	Working register group selection bit: RS1 / RS0 / Currently selected working register group (0 to 3) 0 / 0 / Group 0 (00H–07H) 0 / 1 / Group 1 (08H–0FH) 1 / 0 / Group 2 (10H–17H) 1 / 1 / Group 3 (18H–1FH)
2	**OV**	Overflow flag bit
1	**F1**	F1 flag User-defined flag
0	**P**	Parity flag bit. This flag represents the parity of the number of 1s in accumulator A. 1: The number of 1s in ACC is odd 0: The number of 1s in ACC is even (including zero)

6.2.2.6 Data pointer DPTR (82H, 83H)

The data pointer DPTR is a 16-bit dedicated register, consisting of the lower 8-bit DPL (82H) and the higher 8-bit DPH (83H). DPTR is the only register in the 8051 core microcontroller that traditionally supports direct 16-bit operations, while DPL and DPH can also be accessed individually as bytes.

7 Power supply, Reset, and Clock

7.1 Power supply circuit

The SC92F531X power core integrates BG, LDO, POR, and LVR circuits, enabling reliable operation within a voltage range of 2.4 to 5.5V. Furthermore, the IC includes built-in, calibrated precision voltages of 1.024V, 2.4V, and 2.048V, which can serve as ADC internal reference voltages. Users can Check specific setting details in sector Analog-to-Digital converter ADC.

7.2 Power-On Reset Process

After the SC92F531X powers on and before user application runs, the following process takes place:

- Reset phase
- information retrieval stage
- Normal operation phase

7.2.1 Reset phase

This means the SC92F531X will stay in reset, until the voltage supplied to it exceeds a certain threshold, after which the internal clock starts effectively. The reset phase duration depends on the external power supply rise time. The reset phase completes only after the supply voltage reaches the internal POR threshold.

7.2.2 information retrieval stage

The SC92F531X contains a warm-up counter internally. During the reset phase, the warm-up counter is held at zero. When the supply voltage exceeds the POR threshold, the internal RC oscillator starts oscillating and the warm-up counter begins counting. When the warm-up counter reaches a certain value, data is read from the IFB (including Code Option) in Flash ROM every fixed number of HRC clock cycles and loaded into the internal system registers. The reset state is released after the warm-up is complete.

7.2.3 Normal operation phase

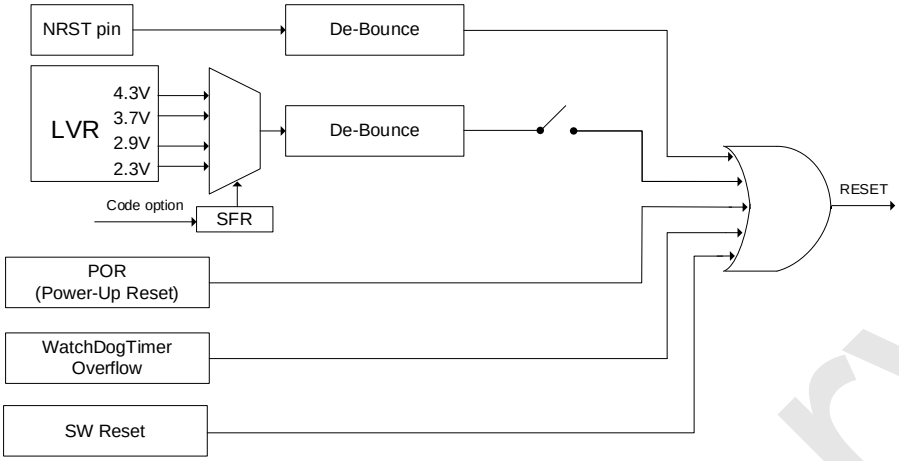
After completing the information retrieval stage, the SC92F531X begins fetching instruction codes from Flash and enters the normal operation phase. The LVR voltage value at this time is the user-set value configured in the Code Option.

7.3 Reset Types

SC92F531X has 5 reset types, the first four are hardware resets:

1. External RST Reset
2. Low Voltage Reset (LVR)
3. Power-On Reset (POR)
4. Watchdog Timer (WDT) Reset
5. Software Reset

The schematic of the reset circuit section of SC92F531X is as follows:



SC92F531X Reset Circuit Diagram

7.3.1 External RST Reset

External RST reset involves applying a reset pulse of a certain width from an external NRST to reset the SC92F531X.

Before programming, users can configure the Customer Option item via the programming software to set pin P1.1 as NRST (reset pin).

7.3.2 Low Voltage Reset (LVR)

The SC92F531X features a built-in low voltage reset circuit. There are four selectable reset threshold voltages: 4.3V, 3.7V, 2.9V, and 2.3V, with the default being the user-written Option value. When the V_{DD} falls below the low voltage reset threshold for longer than T_{LVR}, a reset will be triggered. T_{LVR} is the debounce time for LVR, approximately 30 μs.

OP_CTM0 (C1H@FFH) Customer Option register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENWDT	DRV_EH	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
Read/Write	R/W	R/W	R/W		R/W	R/W	R/W	
Power-On Initial Value	n	n	n		n	n	n	

Bit Number	Bit Symbol	Description
2	**DISLVR**	LVR enable setting 0: LVR enabled normally 1: LVR disabled
1-0	**LVRS [1:0]**	LVR Voltage Selection Control 11: 4.3 V reset 10: 3.7V Reset 01: 2.9V Reset 00: 2.3V Reset

7.3.3 Power-On Reset (POR)

The SC92F531X has an internal Power-On Reset circuit that automatically resets the system when the power supply voltage V_{DD} reaches the POR reset voltage.

7.3.4 Watchdog Reset WDT

The SC92F531X includes a WDT whose clock source is an internal 32 kHz oscillator. The user can select whether to enable the watchdog reset function via the programmer's Code Option settings.

OP_CTM0 (C1H@FFH) Customer Option register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENWDT	DRV_EH	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
Read/Write	R/W	R/W	R/W		R/W	R/W	R/W	
Power-On Initial Value	n	n	n		n	n	n	

Bit Number	Bit Symbol	Description
7	**ENWDT**	WDT enable bit (this bit is loaded by the system according to the user's Code Option setting) 1: WDT starts working 0: WDT disabled

WDTCON (CFH) Watchdog control register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	CLRWDT	-	WDTCKS[2:0]		
Read/Write	-	-	-	R/W	-	R/W		
Power-On Initial Value	x	x	x	0	x	0	0	0

Bit Number	Bit Symbol	Description
4	**CLRWDT**	WDT clear bit (write 1 to clear) 1: WDT counter starts counting from 0 This bit is automatically cleared to 0 by system hardware
2-0	**WDTCKS [2:0]**	Watchdog clock selection WDTCKS[2:0] / WDT overflow time 000 / 500ms 001 / 250ms 010 / 125ms 011 / 62.5ms 100 / 31.5ms 101 / 15.75ms 110 / 7.88ms 111 / 3.94ms
7-5，3	**-**	Reserved

7.3.5 Software Reset

PCON (87h) Power management control register (W, *not readable*)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SMOD	-	-	-	RST	-	STOP	IDL
Read/Write	W	-	-	-	W	-	W	W
Power-On Initial Value	0	x	x	x	n	x	0	0

Bit Number	Bit Symbol	Description
3	**RST**	Software reset control bit: Write status: 0: Program operating normally 1: Writing “1” to this bit causes the CPU to immediately reset

7.3.6 Reset initial state

When the SC92F531X is in Reset state, most registers return to their initial values. The watchdog WDT is disabled. The program counter (PC) initial value is 0000h, and the stack pointer (SP) initial value is 07h. 'Warm reset' (such as WDT, LVR, software reset) do not affect SRAM the SRAM content always remains the same as before reset. Loss of SRAM content occurs when the power supply voltage drops below the level at which RAM can retain data.

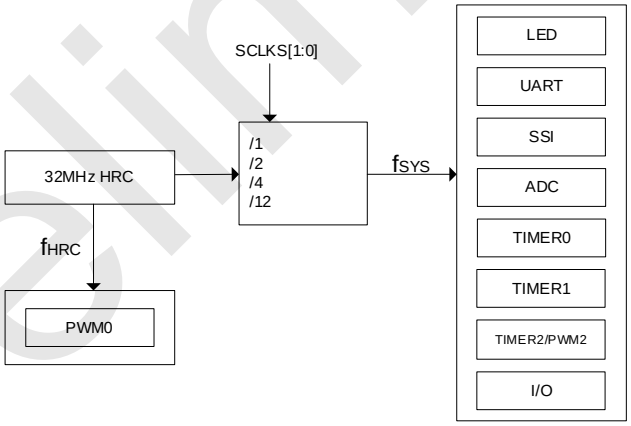
The initial values of SFR registers after Power-On Reset see SFR Description for details.

7.4 High-frequency system clock circuit

The SC92F531X features a built-in high-precision HRC with an adjustable oscillator frequency. The HRC is factory-calibrated to 32 MHz@5V/25 °C. Users can configure the system clock to 32, 16, 8, or 2.66 MHz via the programmer's Code Option. This calibration process compensates for process variations to ensure accuracy.

This HRC exhibits certain drift influenced by operating temperature and voltage:

- Frequency drift over voltage (2.4 V to 5.5 V) and temperature (-40 °C to 85 °C) is typically within ±1%.
- Frequency drift over voltage (2.4 V to 5.5 V) and temperature (-40 °C to 105 °C) is typically within ±1.5%.



Internal Clock Relationship of SC92F531X

OP_CTM0 (C1h@FFH) Customer Option register 0 (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ENWDT	DRV_EH	SCLKS[1:0]		DISRST	DISLVR	LVRS[1:0]	
Read/Write	R/W	R/W	R/W		R/W	R/W	R/W	
Power-On Initial Value	n	n	n		n	n	n	

Bit Number	Bit Symbol	Description
5-4	**SCLKS[1:0]**	System clock frequency selection: 00: System clock frequency equals High-Frequency Oscillator

Bit Number	Bit Symbol	Description
		frequency divided by 1 01: System clock frequency equals High-Frequency Oscillator frequency divided by 2 10: System clock frequency equals High-Frequency Oscillator frequency divided by 4 11: System clock frequency equals High-Frequency Oscillator frequency divided by 12.

The SC92F531X features a special function allowing users to modify SFR values to adjust the HRC frequency within a certain range. This can be done by configuring the OP_HRCR register. Refer to the chapter for the configuration method:Option related SFR operation description.

OP_HRCR (83H@FFH) System clock change register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	OP_HRCR[5:0]					
Read/Write	-	-	R/W					
Power-On Initial Value	x	x	n	n	n	n	n	n

Bit Number	Bit Symbol	Description
5-0	**OP_HRCR[5:0]**	**HRC frequency adjustment register** The center value 1000 0000b corresponds to the HRC center frequency increasing this value increases the frequency, while decreasing it lowers the frequency. Users can modify the value of this register to change the high-frequency oscillator frequency f_{HRC}, thereby adjusting the IC's system clock frequency f_{SYS}: 1. The initial power-on value OP_HRCR[5:0], denoted OP_HRCR[s], is fixed to ensure f_{HRC} is 32 MHz, though the OP_HRCR[s] value may vary between individual ICs 2. With the initial OP_HRCR setting, the IC's system clock frequency f_{SYS} can be precisely set to 32/16/8/2.66 MHz through Option items, and each increment of OP_HRCR[5:0] changes f_{SYS} by approximately 0.5%. The relationship between OP_HRCR [5:0] and f_{SYS} output frequency is as follows:

OP_HRCR [5:0] value	f_{SYS} actual output frequency (using 32 MHz as an example)
OP_HRCR [s]-n	32000*(1-0.5%*n)kHz
...	....
OP_HRCR [s]-2	32000*(1-0.5%*2)= 31680 kHz
OP_HRCR [s]-1	32000*(1-0.5%*1)= 31840 kHz
OP_HRCR [s]	32000 kHz
OP_HRCR [s]+1	32000*(1+0.5%*1)= 32160 kHz
OP_HRCR [s]+2	32000*(1+0.5%*2)= 32320 kHz
...	...
OP_HRCR [s]+n	32000*(1+0.5%*n)kHz

Note:

Bit Number	Bit Symbol	Description
		1. After each power-on, the IC sets OP_HRCR [5:0] to the High-Frequency Oscillator frequency f_{HRC} closest to 32 MHz **2. To ensure reliable IC operation, the maximum operating frequency should preferably not exceed 10% above 32 MHz, i.e., 35.2 MHz** **3. Ensure that changing the HRC frequency will not affect other functions.**

7.5 Low Frequency Oscillator and Low Frequency Clock Timer

The SC92F531X has a built-in 32 kHz RC oscillator that serves as the clock source for the low frequency clock timer (Base Timer) and WDT. Starting the Base Timer or enabling the WDT will both start the 32 kHz Low Frequency Oscillator.

The Low Frequency Clock Timer Base Timer can wake the CPU from STOP mode and generate Interrupts.

BTMCON (CEH) Low Frequency Timer Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ENBTM	BTMIF	-	-	BTMFS[3:0]			
Read/Write	R/W	R/W	-	-	R/W			
Power-On Initial Value	0	0	x	x	0	0	0	0

Bit Number	Bit Symbol	Description
7	**ENBTM**	Low Frequency Base Timer Start Control 0: Base Timer does not start 1: Base Timer starts
6	**BTMIF**	Base Timer Interrupt Request Flag This flag is automatically cleared by hardware when the CPU accepts the Base Timer Interrupt.
3-0	**BTMFS [3:0]**	Low-frequency Clock Interrupt Frequency Selection 0000: Interrupt every 15.625 ms 0001: Interrupt every 31.25 ms 0010: Interrupt every 62.5 ms 0011: Interrupt every 125 ms 0100: Interrupt every 0.25 s 0101: Interrupt every 0.5 s 0110: Interrupt every 1.0 s 0111: Interrupt every 2.0 s 1000: Interrupt every 4.0 s 1001: Interrupt every 8.0 s 1010: Interrupt every 16.0 s 1011: Interrupt every 32.0 s 1100-1111: Reserved
5-4	**-**	Reserved

7.6 STOP mode and IDLE Mode

The SC92F531X provides a Special Function Register PCON configuring bit0 and bit1 of this register controls MCU entry into different Operating Modes.

Writing 1 to PCON.1 stops the internal high-frequency system clock, entering STOP mode. In STOP mode, the user can wake SC92F531X via external interrupts INT0-1, low-frequency clock interrupts, or by external Reset.

Writing 1 to PCON.0 stops program execution and enters IDLE mode, while peripherals and clocks continue running. All CPU state is saved before entering IDLE mode. IDLE mode can be woken up by any interrupt.

PCON (87H) Power supply management control register (W, *not readable*)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SMOD	-	-	-	RST	-	STOP	IDL
Read/Write	W	-	-	-	W	-	W	W
Power-On Initial Value	0	x	x	x	n	x	0	0

Bit Number	Bit Symbol	Description
1	**STOP**	STOP mode control 0: Normal operation mode 1: Power-saving mode where the High-Frequency Oscillator stops working, and the Low Frequency Oscillator and WDT can be optionally enabled based on configuration.
0	**IDL**	IDLE mode control 0: Normal operation mode 1: Power-saving mode where program execution stops, but external devices and clocks continue operating. All CPU status is saved before entering IDLE mode.

Note: When entering STOP or IDLE mode, the instruction that sets the PCON register must be followed by 8 NOP instructions. No other instructions should be placed immediately after; otherwise, subsequent instructions may not execute correctly after wake-up.

For detailed examples, users can refer to the “SC92F_Lib” file.

8 Central Processing Unit CPU and instruction set

8.1 CPU

The SC92F531X uses a standard 8051 CPU core with an instruction set fully compatible with the traditional 8051 family.

8.2 Addressing modes

The addressing modes of the SC92F531X 8051 CPU instructions include: ① Immediate addressing ② Direct addressing ③ Indirect addressing ④ Register addressing ⑤ Relative addressing ⑥ Indexed addressing ⑦ Bit addressing

8.2.1 Immediate addressing

Immediate addressing, also called immediate operand addressing, directly specifies the operand within the instruction. Example:

MOV A, #50H This instruction loads the immediate value 50H into Accumulator A.

8.2.2 Direct addressing

In direct addressing mode, the instruction operand field specifies the address of the operand involved in the operation. Direct addressing mode can only represent SFRs, internal data registers, and bit address space. Among these, SFRs and the bit address space can only be accessed through direct addressing mode. Examples are as follows:

ANL 50H, #91H (ANDs content at address 50H with 91H, result stored at 50H. 50H is a direct address in internal data RAM)

8.2.3 Indirect addressing

Indirect addressing is indicated by adding the '@' symbol before R0 or R1. Assuming the data in R1 is 40H, and the data in internal memory cell 40H is 55H, then:

MOV A, @R1 (move the data 55H to Accumulator A).

8.2.4 Register addressing

Register addressing operates on the selected working registers R7-R0, accumulator A, general-purpose register B, DPTR, and carry flag C. Registers R7-R0 are represented by the low 3 bits of the opcode, while ACC, B, DPTR, and the carry flag C are implicit in the opcode. Therefore, register addressing also includes an implicit addressing mode. The selection of the register workspace is determined by RS1 and RS0 bits in the Program Status Word register (PSW). The registers specified by instruction operands always refer to registers in the current workspace.

INC R0 means (R0) + 1 → R0

8.2.5 Relative addressing

Relative addressing adds an offset to the program counter (PC). The offset is specified in the second byte of the instruction. The result becomes the branch target address. Because the destination address is relative to the PC's base address, this addressing mode is called relative addressing. The offset is a signed number with a range of +127 to -128. This addressing mode is primarily used for branch instructions.

JC $+50H

Indicates that if the carry flag C is 0, the content of the program counter PC remains unchanged, meaning no branch occurs. If the carry flag C is 1, the destination address of the branch instruction is calculated by adding the current PC value, the base address, and the offset 50H.

8.2.6 Indexed addressing

In indexed addressing mode, the instruction operand specifies an index register that holds the base address. During indexed addressing, the offset is added to the base value in the index register; the result is used as the operand address. Index registers include the program counter (PC) and the address register (DPTR).

MOVC A, @A+DPTR

Indicates that accumulator A serves as an offset register. Its contents are added to the contents of the address register DPTR, and the resulting address is used to fetch data, which is then loaded into accumulator A.

8.2.7 Bit addressing

Bit addressing refers to the addressing mode used to perform bit operations on certain internal data Memory (RAM) and SFRs that allow bit manipulation. During bit operations, the carry bit C functions as the accumulator, and the instruction operand directly specifies the bit address. Then, the bit is manipulated according to the opcode type. Bit address encoding matches byte direct addressing encoding, primarily differentiated by the operation type. Care must be taken to distinguish bit from byte operations.

MOV C, 20H (Transfer the value of the bit-addressable register at address 20H to the carry bit C.)

9 INTERRUPT

The SC92F531X offers 11 interrupt sources: Timer0-2, INT0-1, ADC, PWM, UART0, SSI, Base Timer, and CMP. These 11 interrupt sources are divided into two priority levels, each of which can be individually configured as high priority or low priority. The two external interrupts can be configured independently to trigger on rising edge, falling edge, or dual-edge. Each interrupt has its own priority setting bit, interrupt flag, interrupt vector, and enable bit. The global interrupt enable bit EA controls whether all interrupts are enabled or disabled.

9.1 Interrupt sources and vectors

The list of interrupt sources, interrupt vectors, and related control bits of the SC92F531X are as follows:

Interrupt source	Trigger condition	Interrupt flag	Interrupt enable control	Interrupt priority control	Interrupt vector	Query priority	Interrupt number (C51)	Flag clear mode	Can wake up from STOP mode
INT0	External interrupt 0 condition met	IE0	EINT0	IPINT0	0003H	1 (High)	0	H/W Auto	Yes
Timer0	Timer0 overflow	TF0	ET0	IPT0	000BH	2	1	H/W Auto	No
INT1	External interrupt 1 condition met	IE1	EINT1	IPINT1	0013H	3	2	H/W Auto	Yes
Timer1	Timer1 overflow	TF1	ET1	IPT1	001BH	4	3	H/W Auto	No
UART	Reception or transmission finished	RI/TI	EUART	IPUART	0023H	5	4	User must clear	No
Timer2	Timer2 overflow	TF2	ET2	IPT2	002BH	6	5	User must clear	No
ADC	ADC conversion complete	ADCIF	EADC	IPADC	0033H	7	6	User must clear	No
SSI	Reception or transmission finished	SPIF/TWIF	ESSI	IPSSI	003BH	8	7	User must clear	No
PWM0	PWM0 overflow	PWMIF	EPWM	IPPWM	0043H	9	8	User must clear	No
BTM	Base Timer overflow	BTMIF	EBTM	IPBTM	004BH	10	9	H/W Auto	Yes
CMP	Comparator interrupt condition met	CMPIF	ECMP	IPCMP	0063H	11	12	User must clear	Yes

When EA=1 and each interrupt enable bit is set to 1, the interrupt occurrences are as follows:

Timer Interrupt: When Timer0 and Timer1 overflow, interrupts are generated and the interrupt flags TF0 and TF1 are set to "1". When the microcontroller executes these timer interrupts, the interrupt flags TF0 and TF1 are

automatically cleared to "0" by hardware. When Timer2 overflows, an interrupt is generated and the interrupt flag TF2 is set to "1". After executing a Timer2 interrupt, hardware does not automatically clear the TF2. This bit must be cleared by the software.

ADC interrupt: The ADC interrupt is triggered when the conversion is complete, and the interrupt flag is the conversion completion flag ADCIF (ADCCON.5). After the user starts the conversion (sets the ADCS bit), if the interrupt is enabled, the interrupt will trigger upon conversion completion. Upon entering the interrupt service routine, the ADCIF flag must be cleared by software.

SSI interrupt: When the SSI completes receiving or sending a frame of data, the SPIF/TWIF bit is automatically set to "1" by hardware, generating the SSI interrupt. When the microcontroller executes this SSI interrupt, the interrupt flag SPIF/TWIF must be cleared by software.

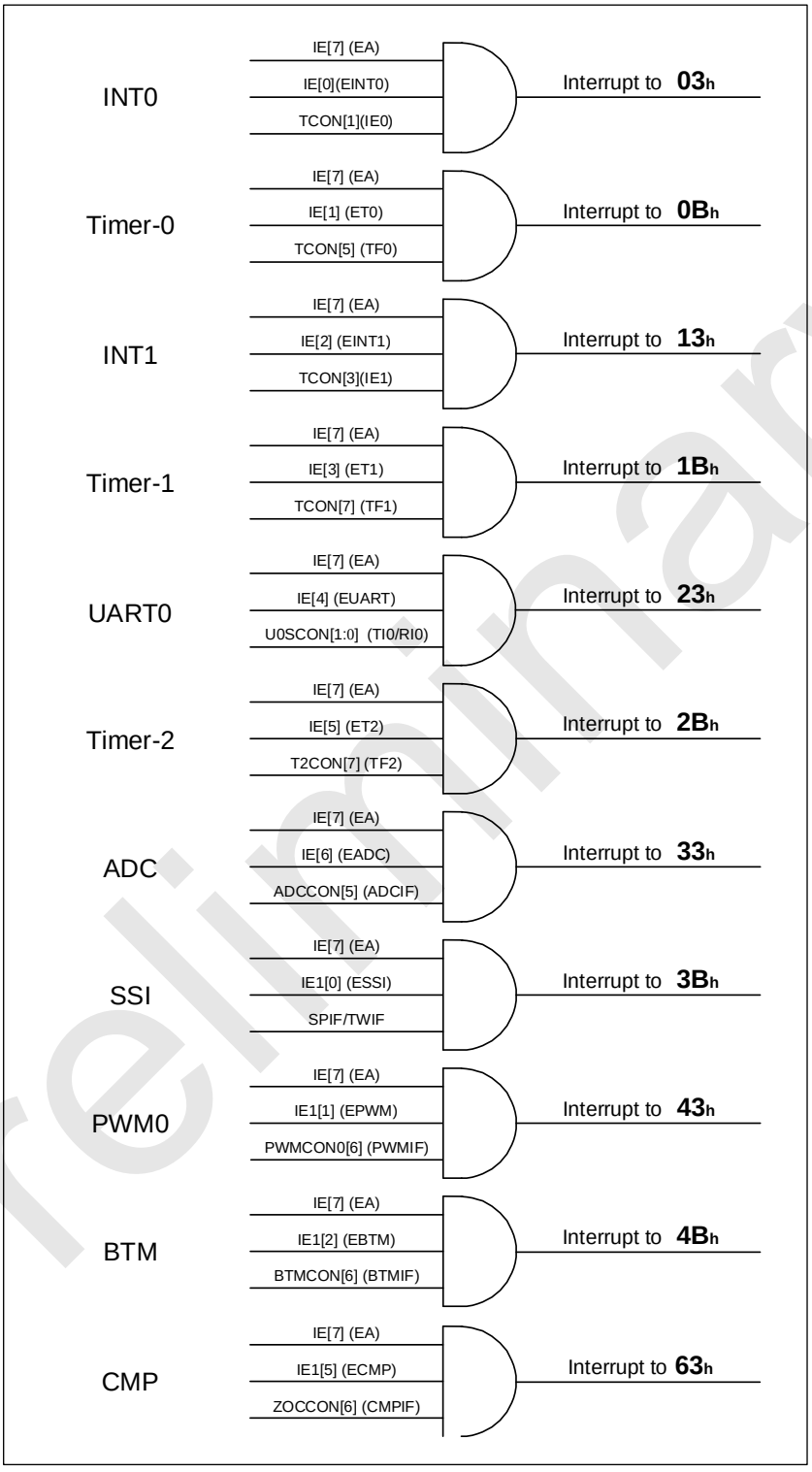
PWM0 interrupt: When the PWM0 counter overflows (that is, the counter reaches PWMPRD), the PWMIF bit (PWM Interrupt Flag) is automatically set to "1" by hardware, generating the PWM0 interrupt. When the PWM0 interrupt occurs and the user enters the interrupt service routine, it must be cleared through software.

External interrupts INT0-1: When an interrupt condition occurs at the external interrupt pin, the external interrupt is triggered. INT0 has 6 external interrupt sources, and INT1 also has 6 external interrupt sources. Users can configure them as rising edge, falling edge, or dual-edge interrupts by setting the SFRs (INTxF and INTxR). Interrupt priority levels can be set via the IP register for each interrupt. External interrupts INT0-1 can also wake the microcontroller from STOP mode.

CMP interrupt: When CMP matches the interrupt conditions set by CMPIM[1:0], the CMPIF bit is automatically set to "1" by hardware, generating the CMP interrupt. After the CMP interrupt has occurred, the interrupt flag CMPIF must be cleared by the software.

9.2 Interrupt structure diagram

The interrupt structure of the SC92F531X is shown in the diagram below:



SC92F531X interrupt structure and vectors

9.3 Interrupt priority

The SC92F663X supports two interrupt priority levels. Interrupt sources can be programmed as either high-priority or low-priority interrupts, allowing two-level nesting of interrupt service routines. A low-priority interrupt in progress can be interrupted by a high-priority interrupt. However, it cannot be interrupted by another interrupt of the same priority. It will execute until completion. After executing the return instruction RETI and returning to the main program, one more instruction must be executed before new interrupt requests can be serviced.

Specifically:

1. A low-priority interrupt can be interrupted by a high-priority interrupt request, but not the other way around During the response to any interrupt, it cannot be interrupted by an interrupt request of the same priority.
2. Any interrupt cannot be interrupted by another interrupt request of the same priority while being serviced.
3. For same-priority interrupts occurring simultaneously, the response priority follows the natural priority order. Interrupts with lower query numbers are serviced first.

9.4 Interrupt handling procedure

When an interrupt occurs and is acknowledged by the CPU, the main program execution is suspended and the following steps are performed:

1. Complete the currently executing instruction
2. Push PC value onto the stack to save the current context
3. Load the interrupt vector address into PC
4. Execute the corresponding interrupt service routine
5. End the interrupt service routine with RETI
6. Pop PC value from stack and resume interrupted program.

During this process, interrupts of the same priority are queued and serviced after current interrupt service routine completes.

9.5 Interrupt-related SFR registers

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**EA**	Global interrupt enable control 0: Disable all interrupts 1: Enable all interrupts
6	**EADC**	ADC interrupt enable control 0: Disable ADC interrupt 1: Enable interruption upon ADC conversion completion
5	**ET2**	Timer 2 interrupt enable control 0: Disable Timer 2 interrupt 1: Enable Timer 2 interrupt
4	**EUART**	UART interrupt enable control

Bit Number	Bit Symbol	Description
		0: Disable UART interrupt 1: Enable UART interrupt
3	**ET1**	Timer 1 interrupt enable control 0: Disable Timer 1 interrupt 1: Enable Timer 1 interrupt
2	**EINT1**	External interrupt 1 enable control 0: Disable INT1 Interrupt 1: Enable INT1 Interrupt
1	**ET0**	Timer 0 interrupt enable control 0: Disable Timer 0 Interrupt 1: Enable Timer 0 Interrupt
0	**EINT0**	External interrupt 0 enable control 0: Disable INT0 Interrupt 1: Enable INT0 Interrupt

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	IPADC	IPT2	IPUART	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
6	**IPADC**	ADC interrupt priority selection 0: ADC interrupt priority is low 1: ADC interrupt priority is high
5	**IPT2**	Timer 2 interrupt priority selection 0: Timer 2 interrupt priority is low 1: Timer 2 interrupt priority is high
4	**IPUART**	UART interrupt priority selection 0: UART interrupt priority is low 1: UART interrupt priority is high
3	**IPT1**	Timer 1 interrupt priority selection 0: Timer 1 interrupt priority is low 1: Timer 1 interrupt priority is high
2	**IPINT1**	INT1 counter interrupt priority selection 0: INT1 interrupt priority is low 1: INT1 interrupt priority is high
1	**IPT0**	Timer 0 interrupt priority selection 0: Timer 0 interrupt priority is low 1: Timer 0 interrupt priority is high
0	**IPINT0**	INT0 counter interrupt priority selection 0: INT0 interrupt priority is low 1: INT0 interrupt priority is high
7	**-**	Reserved

IE1 (A9H) Interrupt Control Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	ECMP	-	-	EBTM	EPWM	ESSI
Read/Write	-	-	R/W	-	-	R/W	R/W	R/W
Power-On Initial Value	x	x	0	x	x	0	0	0

Bit Number	Bit Symbol	Description
5	**ECMP**	CMP interrupt enable control 0: Disable CMP interrupt 1: Enable CMP interrupt
2	**EBTM**	Base Timer interrupt enable control 0: Disable Base Timer interrupt 1: Enable Base Timer interrupt
1	**EPWM**	PWM interrupt enable control 0: Disable PWM0 interrupt 1: Enable PWM0 interrupt when counter overflows (reaches PWMPRD)
0	**ESSI**	SSI interrupt enable control 0: Disable SSI interrupt 1: Enable SSI interrupt

IP1 (B9H) Interrupt Priority Control Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	IPCMP	-	-	IPBTM	IPPWM	IPSSI
Read/Write	-	-	R/W	-	-	R/W	R/W	R/W
Power-On Initial Value	x	x	0	x	x	0	0	0

Bit Number	Bit Symbol	Description
5	**IPCMP**	CMP interrupt priority selection 0: CMP interrupt priority is low 1: CMP interrupt priority is high
2	**IPBTM**	Base Timer interrupt priority selection 0: Base Timer interrupt priority is low 1: Base Timer interrupt priority is high
1	**IPPWM**	PWM interrupt enable selection 0: PWM0 interrupt priority is low 1: PWM0 interrupt priority is high
0	**IPSSI**	Three-way communication port SSI interrupt priority selection 0: SSI interrupt priority is low 1: SSI interrupt priority is high

TCON (88H) Timer Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Power-On Initial Value	0	0	0	0	0	x	0	x

Bit Number	Bit Symbol	Description
3	**IE1**	External interrupt 1 request flag 0: No interrupt pending

Bit Number	Bit Symbol	Description
		1: External interrupt 1 request detected (set by hardware on edge detection). Automatically cleared by hardware when the CPU services the interrupt.
1	**IE0**	External interrupt 0 request flag 0: No interrupt pending 1: External interrupt 0 request detected (set by hardware on edge detection). Automatically cleared by hardware when the CPU services the interrupt.
2，0	**-**	Reserved

INT0F (BAH) INT0 falling edge Interrupt control register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	-	INT0F5	INT0F4	INT0F3	INT0F2	INT0F1	INT0F0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5-0	**INT0Fn (n=0-5)**	INT0 falling edge interrupt control 0: Disable INT0n falling edge interrupt 1: Enable INT0n falling edge interrupt

INT0R (BBH) INT0 rising edge Interrupt control register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	-	INT0R5	INT0R4	INT0R3	INT0R2	INT0R1	INT0R0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5-0	**INT0Rn (n=0-5)**	INT0 rising edge interrupt control 0: Disable INT0n rising edge interrupt 1: Enable INT0n rising edge interrupt

INT1F (BCH) INT1 falling edge Interrupt control register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	-	INT1F5	INT1F4	INT1F3	INT1F2	INT1F1	INT1F0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5-0	**INT1Fn (n=0-5)**	INT1 falling edge interrupt control 0: Disable INT1n falling edge interrupt 1: Enable INT1n falling edge interrupt

INT1R (BDH) INT1 rising edge Interrupt control register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	INT1R5	INT1R4	INT1R3	INT1R2	INT1R1	INT1R0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5-0	**INT1Rn (n=0-5)**	INT1 rising edge Interrupt control 0: Disable INT1n rising edge interrupt 1: Enable INT1n rising edge interrupt

10 TIMER0, TIMER1

The SC92F531X contains two 16-bit timers/counters, each featuring two operating modes: counting mode and timing mode. The TMOD includes a control bit C/Tx to select whether T0 and T1 operate as timers or counters. They are essentially incremental counters, differing only in their count source. The timer counts are driven by the system clock or its divided clock, while the counter counts are driven by input pulses from external pins. T0 and T1 start counting only when TRx=1.

In counter mode, each pulse on the P1.2/T0 and P1.3/T1 pins increases the count value of T0 and T1 by 1 respectively.

In timer mode, the count source for T0 and T1 can be selected via the TMCON as $f_{SYS}/12$ or f_{SYS} (f_{SYS} is the system clock frequency).

Timer/Counter T0 has 4 operating modes, while Timer/Counter T1 has 3 operating modes (mode 3 is unavailable):

1. Mode 0: 13-bit Timer/Counter mode
2. Mode 1: 16-bit Timer/Counter mode
3. Mode 2: 8-bit Auto-Reload mode
4. Mode 3: Two 8-bit Timer/Counter mode

For the above modes, modes 0, 1, and 2 of T0 and T1 are the same, while mode 3 differs.

10.1 Special Function Registers Related to T0 and T1

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
TCON	88H	Timer Control Register	TF1	TR1	TF0	TR0	IE1	-	IE0	-	00000x0xb
TMOD	89H	Timer Operating Mode Register	-	C/T1	M11	M01	-	C/T0	M10	M00	x000x000b
TL0	8AH	Timer 0 Low Byte	TL0[7:0]								00000000b
TL1	8BH	Timer 1 Low Byte	TL1[7:0]								00000000b
TH0	8CH	Timer 0 High Byte	TH0[7:0]								00000000b
TH1	8DH	Timer 1 High Byte	TH1[7:0]								00000000b
TMCON	8EH	Timer Frequency Control Register	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b

The following explains each register:

TCON (88H) Timer Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF1	TR1	TF0	TR0	IE1	-	IE0	-
Read/Write	R/W	R/W	R/W	R/W	R/W	-	R/W	-
Power-On Initial Value	0	0	0	0	0	x	0	x

Bit Number	Bit Symbol	Description
7	**TF1**	T1 overflow interrupt request flag 0: Cleared by hardware when CPU responds to interrupt 1: Set by hardware on T1 overflow
6	**TR1**	Run control bit of Timer T1.

Bit Number	Bit Symbol	Description
		0: Timer 1 counting is disabled 1: Timer 1 starts counting This bit is set and cleared by software.
5	**TF0**	T0 overflow interrupt request flag 0: Cleared by hardware when CPU responds to interrupt 1: Set by hardware on T0 overflow
4	**TR0**	Run control bit of Timer T0 0: Timer 0 counting is disabled 1: Timer 0 starts counting This bit is set and cleared by software.
2，0	**-**	Reserved

TMOD (89H) Timer working mode register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	C/T1	M11	M01	-	C/T0	M10	M00
Read/Write	-	R/W	R/W	R/W	-	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	x	0	0	0
	T1				T0			

Bit Number	Bit Symbol	Description
6	**C/T1**	TMOD[6] controls Timer 1 0: Timer mode, T1 counts from f_{SYS} divided clock 1: Counter mode, T1 counts from external pin T1/P1.3
5-4	**M11,M01**	Timer/Counter 1 mode selection 00: 13-bit Timer/Counter, upper 3 bits of TL1 invalid 01: 16-bit Timer/Counter, TL1 and TH1 fully valid 10: 8-bit auto-reload Timer, on overflow TH1 value is automatically reloaded into TL1 11: Timer/Counter 1 invalid (count stopped)
2	**C/T0**	TMOD[2] controls Timer 0 0: Timer, T0 count source is the f_{SYS} divider 1: Counter, T0 count source is the external pin T0/P1.2
1-0	**M10,M00**	Timer/Counter 0 mode selection 00: 13-bit Timer/Counter, the upper 3 bits of TL0 are invalid 01: 16-bit Timer/Counter, TL0 and TH0 are fully valid 10: 8-bit auto-reload Timer, TH0 value automatically reloads into TL0 upon overflow 11: Timer 0 functions as two 8-bit Timer/CountersTL0 acts as an 8-bit Timer/Counter controlled by standard Timer 0 control bitsTH0 functions only as an 8-bit Timer, controlled by the control bits of Timer1
7，3	**-**	Reserved

In the TMOD register, TMOD[0]-TMOD[2] configure the operating mode of T0 TMOD[4]-TMOD[6] configure the operating mode of T1.

The Timer and Counter Tx function is selected by the C/Tx control bit in the Special Function Register TMOD, while M0x and M1x are used to select Tx's operating mode. TRx acts as the on/off control for T0 and T1 T0 and T1 operate only when TRx = 1.

TMCON (8EH) Timer frequency control register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	T1FD	T0FD
Read/Write	-	-	-	-	-	-	R/W	R/W
Power-On Initial Value	x	x	x	x	x	x	0	0

Bit Number	Bit Symbol	Description
1	**T1FD**	T1 input frequency selection control 0: T1 frequency derived from $f_{SYS}/12$ 1: T1 frequency derived from f_{SYS}
0	**T0FD**	T0 input frequency selection control 0: T0 frequency derived from $f_{SYS}/12$ 1: T0 frequency derived from f_{SYS}
7-2	**-**	Reserved

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
3	**ET1**	Timer 1 Interrupt enable control 0: Disable T1 interrupt 1: Enable T1 interrupt
1	**ET0**	Timer0 Interrupt enable control 0: Disable T0 Interrupt 1: Enable T0 Interrupt

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	IPADC	IPT2	IPUART0	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
3	**IPT1**	Timer1 Interrupt Priority 0: Timer1 interrupt priority is low 1: Timer1 interrupt priority is high
1	**IPT0**	Timer0 Interrupt Priority

Bit Number	Bit Symbol	Description
		0: Timer0 interrupt priority is low 1: Timer0 interrupt priority is high

10.2 T0 operating mode

Timer/Counter 0 supports four different operating modes by setting the M10 and M00 bits (TMOD[1] and TMOD[0]) in the TMOD register.

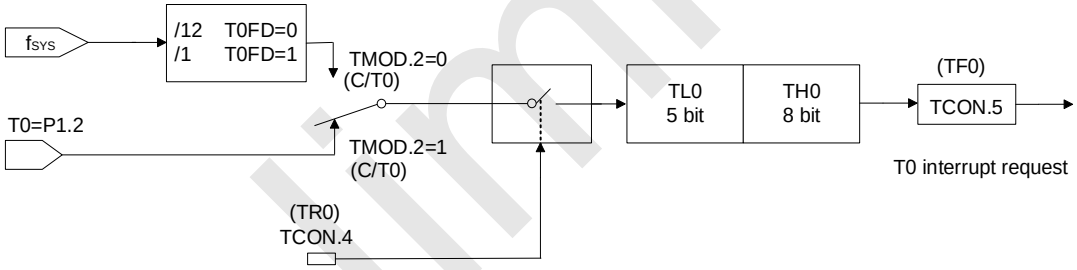
10.2.1 Operating mode 0: 13-bit counter/timer

The TH0 register stores the high 8 bits (TH0.7-TH0.0) of the 13-bit counter/timer, while TL0 stores the low 5 bits (TL0.4-TL0.0). The high three bits of TL0 (TL0.7-TL0.5) are undefined and should be ignored when reading. When the 13-bit timer/counter overflows, the system sets the timer overflow flag TF0 to 1. If the Timer 0 interrupt is enabled, an interrupt will be generated.

The C/T0 bit selects the clock input source for the counter/timer. If C/T0 = 1, a high-to-low transition on the Timer 0 input pin T0 (P1.2) increments the Timer 0 data register by 1. If C/T0=0, the system clock prescale is selected as the clock source for Timer 0.

When TR0 is set to 1, Timer 0 is enabled. Setting TR0 to 1 does not forcibly reset the timer; this means the timer register will continue counting from its value when TR0 was last cleared. Therefore, the initial value of the timer register should be set before enabling the timer.

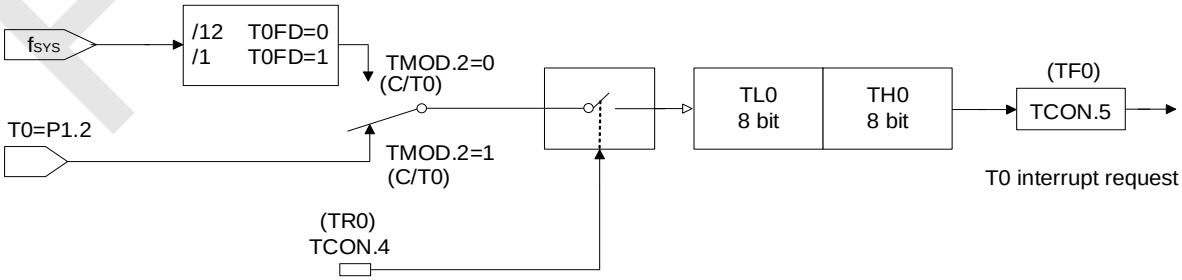
When used as a timer, T0FD can be configured to select the clock source prescale ratio.



Timer/Counter operating mode 0: 13-bit timer/counter

10.2.2 Operating mode 1: 16-bit counter/timer

Except for using the 16-bit counter/timer mode (where all 8 bits of TL0 data are valid), modes 1 and 0 operate similarly. The methods to enable and configure the counter/timer are also the same.



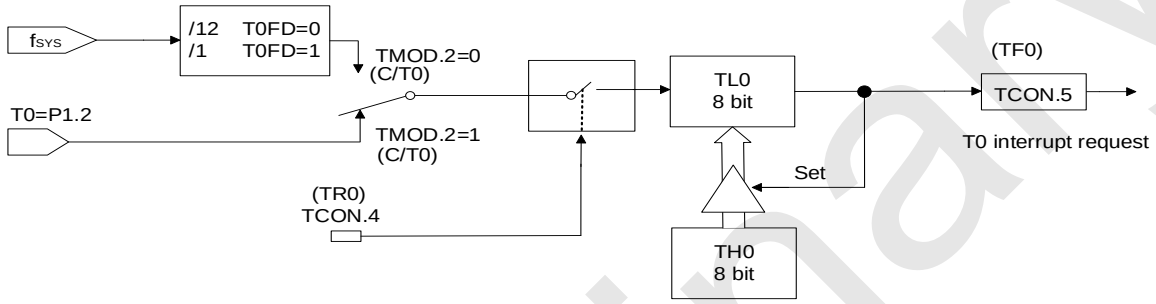
Timer/Counter operating mode 0: 16-bit timer/counter

10.2.3 Operating mode 2: 8-bit auto-reload counter/timer

In operating mode 2, Timer 0 functions as an 8-bit auto-reload counter/timer. TL0 stores the count value, TH0 stores the reload value. When the TL0 counter overflows, the timer overflow flag TF0 is set, and the value in register TH0 is reloaded into TL0. If the Timer interrupt is enabled, an interrupt will be generated when TF0 is set. The reload value in TH0 remains unchanged. Before the timer can start counting properly, TL0 must be initialized to the desired value.

Apart from the automatic reload function, the enable and configuration of the counter/timer in mode 2 are the same as in modes 0 and 1.

When used as a timer, TMCON.0 (T0FD) can be configured to select the timer clock source as a divided portion of the system clock f_{SYS}.



Timer/Counter Operating Mode 2: 8-bit auto-reload timer/counter

10.2.4 Operating mode 3: two 8-bit counters/timers (timer 0 only)

In mode 3, timer 0 is used as two independent 8-bit timers/counters, controlled separately by TL0 and TH0. TL0 is controlled by the control bits of timer 0 (in TCON) and the status bits (in TMOD): TR0, C/T0, and TF0. Timer 0 can be configured to operate in either timer mode or counter mode through T0's TMOD.2 (C/T0) setting.

TH0 is controlled by the TCON register of timer 1; however, TH0 is restricted to timer mode and cannot be switched to counter mode via TMOD.2 (C/T0). TH0 is enabled and controlled by the timer control bit TR1, which must be set to 1. When an overflow occurs, TF1 is set to 1, triggering an interrupt. The corresponding interrupt service for Timer 1 is then executed.

When Timer 0 is configured to operate in mode 3, the TH0 timer uses the interrupt resources and TCON register of Timer 1. Consequently, Timer 1's 16-bit counter stops counting, equivalent to "TR1=0". When using the TH0 timer, TR1 must be set to 1.

10.3 T1 Operating mode

Through the configuration of M11 and M01 (TMOD[5], TMOD[4]) bits in the TMOD register, timer/counter 1 can work in three different operating modes.

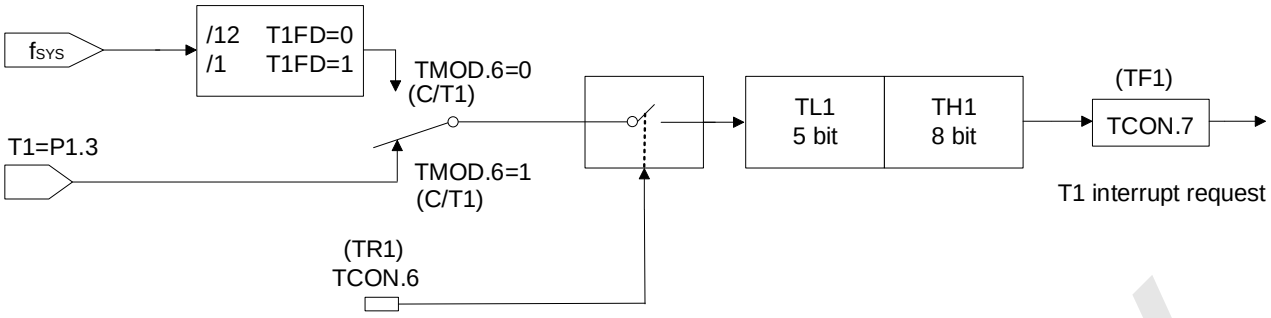
10.3.1 Operating mode 0: 13-bit counter/timer

TH1 holds the high 8 bits (TH1.7 to TH1.0) of the 13-bit counter/timer. TL1 holds the low 5 bits (TL1.4 to TL1.0). The upper three bits of TL1 (TL1.7 to TL1.5) are undefined and should be ignored upon reading. When the 13-bit timer/counter increments and overflows, the system sets the timer overflow flag TF1 to 1. If the Interrupt for Timer 1 is enabled, an interrupt will be generated. The C/T1 bit selects the clock source for the counter/timer.

If C/T1=1, the timer 1 data register increments by 1 on the falling edge of timer 1 input pin T1 (P1.3). If C/T1=0, the clock source for timer 1 is the divided system clock.

Setting TR1 to 1 turns on the timer. Setting TR1 to 1 does not forcibly reset the timer, meaning the timer will resume counting from its value at the last time TR1 was cleared. Therefore, the initial value of the timer register should be set before enabling the timer.

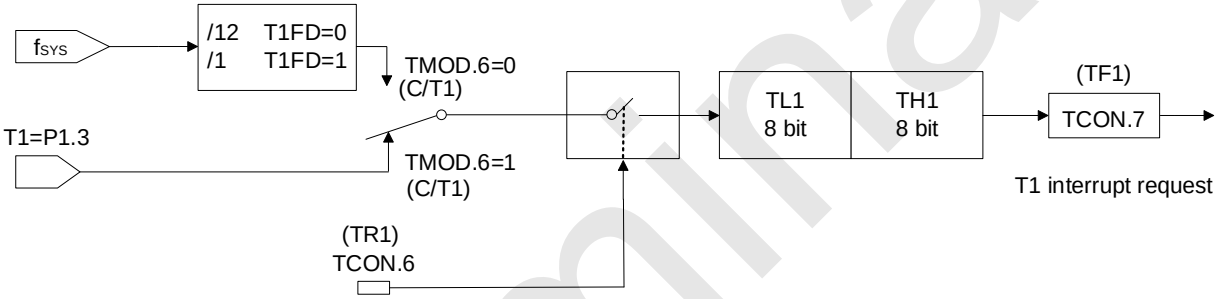
When used as a Timer, T1FD can be configured to select the clock source division ratio.



Timer/Counter operating mode 0: 13-bit timer/counter

10.3.2 Operating mode 1: 16-bit counter/timer

Except for using the 16-bit counter/timer mode (where all 8 bits of TL1 data are valid), modes 1 and 0 operate similarly. The methods to enable and configure the counter/timer are also the same.



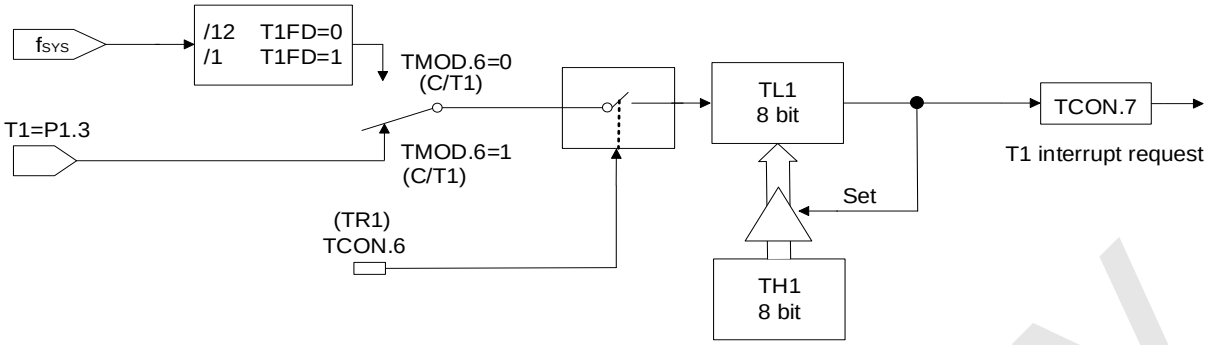
Timer/Counter operating mode 0: 16-bit timer/counter

10.3.3 Operating mode 2: 8-bit auto-reload counter/timer

In operating mode 2, Timer 1 acts as an 8-bit auto-reload counter/Timer. TL 1 holds the count value, while TH1 holds the reload value. When the counter in TL1 overflows to 0x00, the Timer overflow flag TF1 is set, and the value in TH1 is reloaded into TL1. If the timer interrupt is enabled, an interrupt will be generated when TF1 is set to 1. The reload value in TH1 remains unchanged. Before the timer can start counting correctly, TL1 must be initialized with the desired value.

Except for the automatic reload function, the enable and configuration of the counter/timer in operating mode 2 are the same as those in modes 0 and 1.

When used as a timer, TMCON.1 (T1FD) can be configured to select the timer clock source as a divided portion of the system clock f_{SYS}.



Timer/Counter operating mode 2: 8-bit auto-reload timer/counter

11 Timer2

Timer2 inside the SC92F531X has two operating modes: counting mode and timing mode. The T2CON contains a control bit C/T2 that selects timer or counter mode. They are essentially incremental counters, differing only in their count source. The timer counts are driven by the system clock or its divided clock, while the counter counts are driven by input pulses from external pins. TR2 is the control switch for T2 counting in timer/counter mode. T2 will count only when TR2=1.

In counter mode, each pulse on the T2 pin increments the T2 count by 1.

In timer mode, the TMCON can select the T2 counting source as either fSYS/12 or fSYS.

Timer/Counter T2 has 4 operating modes:

1. Mode 0: 16-bit capture mode
2. Mode 1: 16-bit auto-reload timer mode
3. Mode 2: Baud rate generator mode
4. Mode 3: Programmable clock output mode

11.1 T2 related special function registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Reset Value
T2CON	C8H	Timer 2 Control Register	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000b
T2MOD	C9H	Timer 2 Working Mode Register	T2FD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN	0x000000b
RCAP2L	CAH	Timer 2 Reload/Capture Low Byte	RCAP2L[7:0]								00000000b
RCAP2H	CBH	Timer 2 Reload/Capture High Byte	RCAP2H[7:0]								00000000b
TL2	CCH	Timer 2 Low Byte	TL2[7:0]								00000000b
TH2	CDH	Timer 2 High Byte	TH2[7:0]								00000000b
TMCON	8EH	Timer Frequency Control Register	-	-	-	-	-	-	T1FD	T0FD	xxxxxx00b

The following explains each register:

T2CON (C8H) Timer 2 Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**TF2**	Timer 2 overflow flag 0: No overflow (must be cleared by software) 1: Overflow (set by hardware if RCLK = 0 and TCLK = 0)
6	**EXF2**	Flag indicating detection of external event input (falling edge) on T2EX pin 0: No external event detected (must be cleared by software) 1: External event detected (set by hardware if EXEN2 = 1)

Bit Number	Bit Symbol	Description
5	**RCLK**	UART receive clock control bit 0: Receive baud rate generated by Timer 1 1: Timer2 generates receiving baud rate
4	**TCLK**	UART transmit clock control bit 0: Timer1 generates transmitting baud rate 1: Timer2 generates transmitting baud rate
3	**EXEN2**	External event input on T2EX pin (falling edge) used as reload/capture trigger enable/disable control: 0: Ignore events on T2EX pin 1: When Timer2 is not used as UART clock, a falling edge detected on T2EX pin generates a capture or reload
2	**TR2**	Timer2 start/stop control bit 0: Stop Timer2 1: Start Timer2
1	**C/T2**	Timer2 timer/counter mode select bit 2 0: Timer mode, T2 pin used as I/O port 1: Counter mode
0	**CP/RL2**	Capture/Reload mode selection bit 0: 16-bit timer/counter with reload function 1: 16-bit timer/counter with capture function, T2EX as Timer 2 external capture signal input

T2MOD (C9H) Timer 2 Working Mode Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	T2FD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**T2FD**	T2 input frequency select control 0: T2 frequency sourced from f_{SYS}/12 1: T2 frequency sourced from f_{SYS}
1	**T2OE**	Timer 2 output enable bit 0: Set T2 as clock input or I/O port 1: Set T2 as clock output
0	**DCEN**	Decrement counting enable bit 0: Disable Timer 2 as increment/decrement counter. Timer 2 operates only as increment counter 1: Enable Timer 2 as increment/decrement counter
6	**-**	Reserved

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5	**ET2**	Timer 2 interrupt enable control 0: Disable Timer 2 interrupt 1: Enable Timer 2 interrupt

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	IPADC	IPT2	IPUART	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5	**IPT2**	Timer 2 interrupt priority 0: Timer 2 interrupt priority is low 1: Timer 2 interrupt priority is high

11.2 Timer 2 operating mode

Timer 2 operating modes and configurations are as follows:

C/$\overline{T2}$	T2OE	DCEN	TR2	CP/$\overline{RL2}$	RCLK	TCLK	Mode	
	0	X	1	1	0	0	0	16-bit capture
X	0	0	1	0	0	0	1	16-bit auto-reload timer
X	0	1	1	0	0	0		
X	0	X	1	X	1	X	2	Baud rate generator
					X	1		
0	1	X	1	X	0	0	3	For programmable clock only
					1	X	3	Programmable clock output with baud rate generator
					X	1		
X	X	X	0	X	X	X	X	Timer 2 stopped T2EX path remains enabled
1	1	X	1	X	X	X		Not recommended

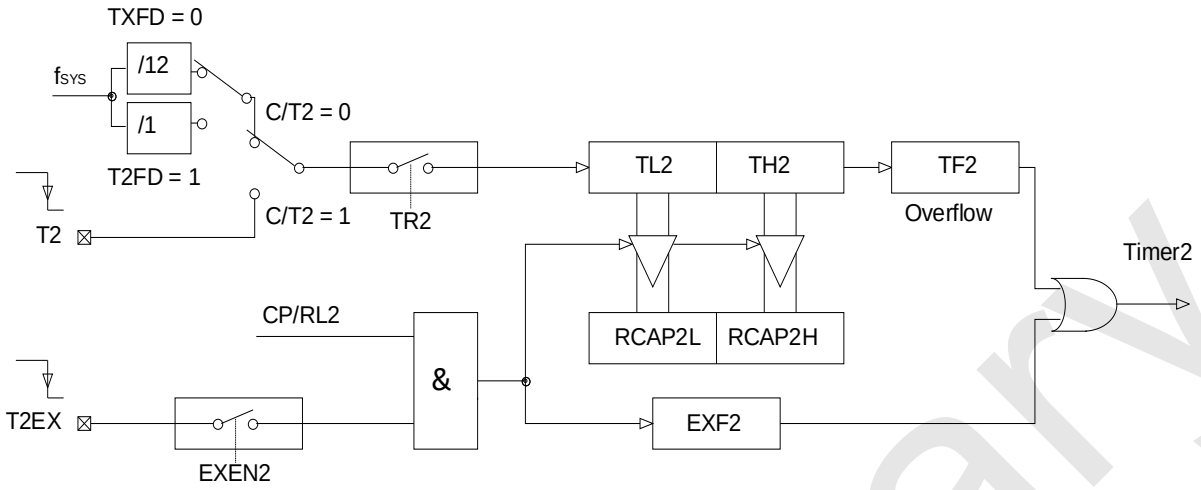
11.2.1 Operating mode 0: 16-bit capture

In capture mode, the EXEN2 bit in T2CON has two options.

When EXEN2 = 0, Timer 2 functions as a 16-bit timer or counter. If ET2 is enabled and the timer overflows, the TF2 is set, which can trigger an interrupt.

When EXEN2 = 1, Timer 2 performs the same operation, but a falling edge on the external T2EX also captures the current values of TH2 and TL2 into RCAP2H and RCAP2L respectively. The falling edge on T2EX

sets the EXF2 bit in T2CON. If ET2 is enabled, EXF2 can trigger an interrupt just like TF2.



Mode 0: 16-bit Capture

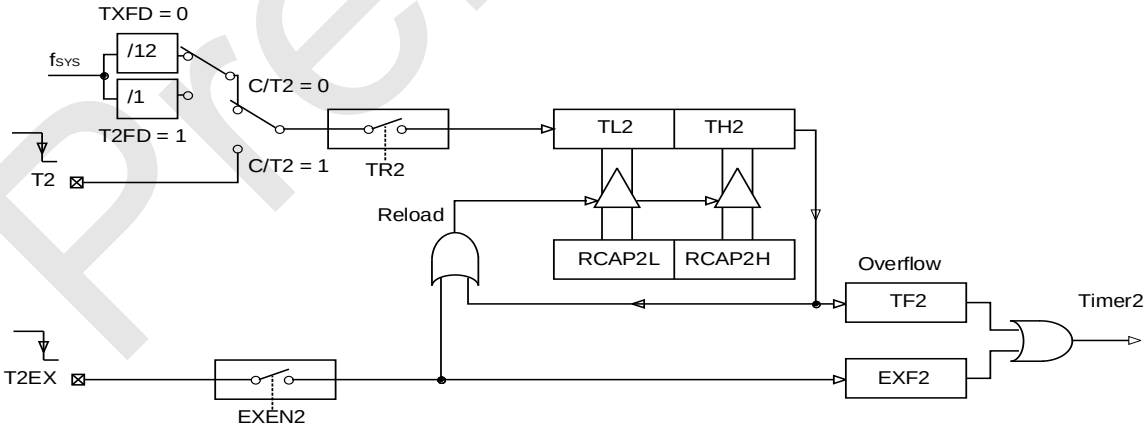
11.2.2 Operating mode 1: 16-bit auto-reload timer

In 16-bit auto-reload mode, Timer 2 supports either incrementing or decrementing count modes, controlled by the DCEN bit in the T2MOD register. After system reset, DCEN defaults to 0, and the timer operates in incrementing counting mode. If DCXEN is set to 1, the counting direction is determined by the level of the T2EX pin.

When DCEN = 0, two options are selected via the EXEN2 bit in the T2CON.

If EXEN2 = 0, the timer increments from the current value to 0xFFFF, then overflows, sets the TF2 flag, and automatically reloads the 16-bit value from RCAP2H and RCAP2L into TH2 and TL2.

If EXEN2 = 1, overflow or the falling edge input on external T2EX can trigger a 16-bit reload. When a falling edge occurs on T2EX, the EXF2 bit is set. If ET2 is enabled, both TF2 and EXF2 bits can generate an interrupt.



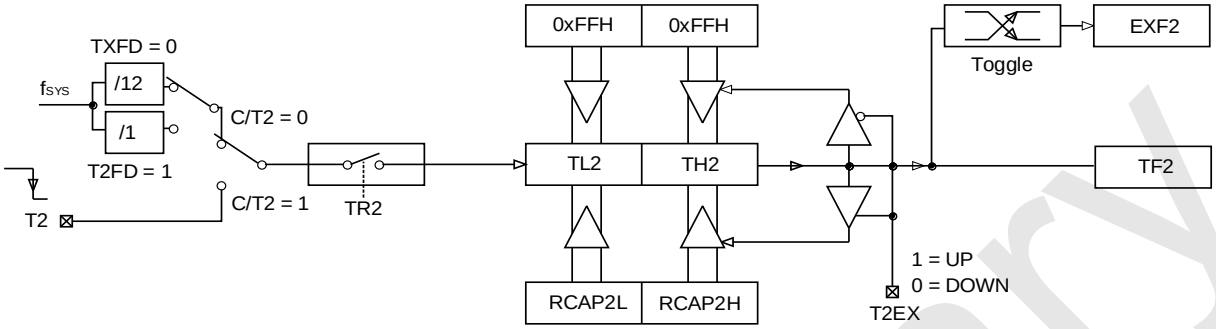
Mode 1: 16-bit auto-reload DCEN = 0

When DCEN = 1, the T2EX pin controls the counting direction, and EXEN2 has no effect.

If the level on T2EX is high, the timer increments the count. When it reaches 0xFFFF, an overflow occurs, triggering TF2, and automatically reloads the initial value from the RCAP2H and RCAP2L registers.

If the level on T2EX is low, the timer decrements the count. When the count value equals the value set in RCAP2H and RCAP2L, an overflow occurs, triggering TFX, and automatically reloads 0xFFFF.

In this mode, the EXF2 bit functions only as the 17th bit of extended counting and does not serve as an interrupt flag.



Mode 1: 16-bit auto-reload DCEN = 1

11.2.3 Operating mode 2: baud rate generator

Timer 2 is selected as the baud rate generator by setting TCLK and/or RCLK bits in the T2CON. The receiver and transmitter can have different baud rates. If Timer 2 is used as the receiver or transmitter baud rate generator, Timer 1 accordingly serves as the baud rate generator for the other.

Set TCLK and/or RCLK bits in the T2CON to configure Timer 2 to operate in baud rate generator mode, which is similar to auto-reload mode.

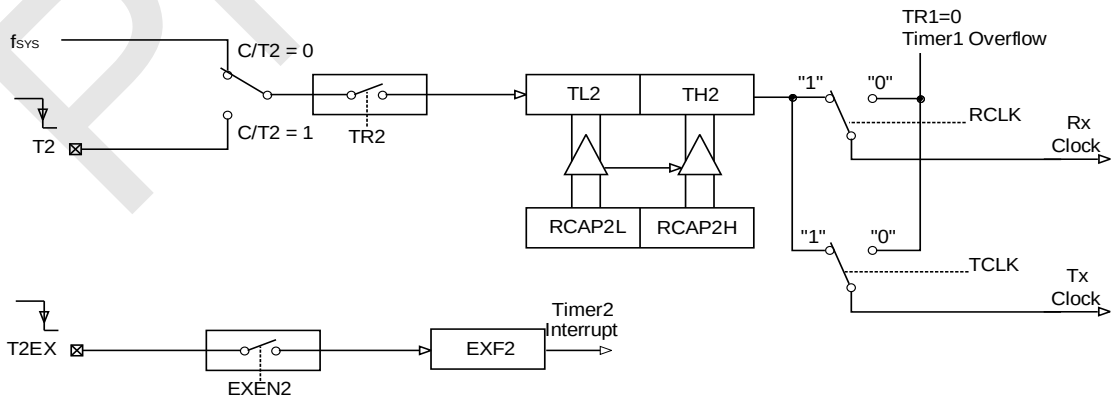
When Timer 2 overflows, the values in the RCAP2H and RCAP2L are reloaded into the Timer 2 counter, but no interrupt is generated.

If EXEN2 is set to 1, a falling edge on the T2EX pin will set EXF2, but will not cause a reload. Thus, when Timer 2 is used as a baud rate generator, T2EX can function as an additional external interrupt.

In UART modes 1 and 3, the baud rate is determined by Timer 2's overflow rate according to the following equation:

$$\text{BaudRate} = \frac{f_{SYS}}{[\text{RCAP2H,RCAP2L}]}$$ (Note: [RCAP2H, RCAP2L] must be greater than 0x0010 **)**

The schematic diagram of Timer 2 as a baud rate generator is as follows:



Mode 2: Baud Rate Generator

11.2.4 Operating mode 3: programmable clock output

In this mode, T2 can be programmed to output a clock signal with a 50% duty cycle: when C/$\overline{T2}$ = 0 and T2OE = 1, Timer 2 is enabled as a clock generator.

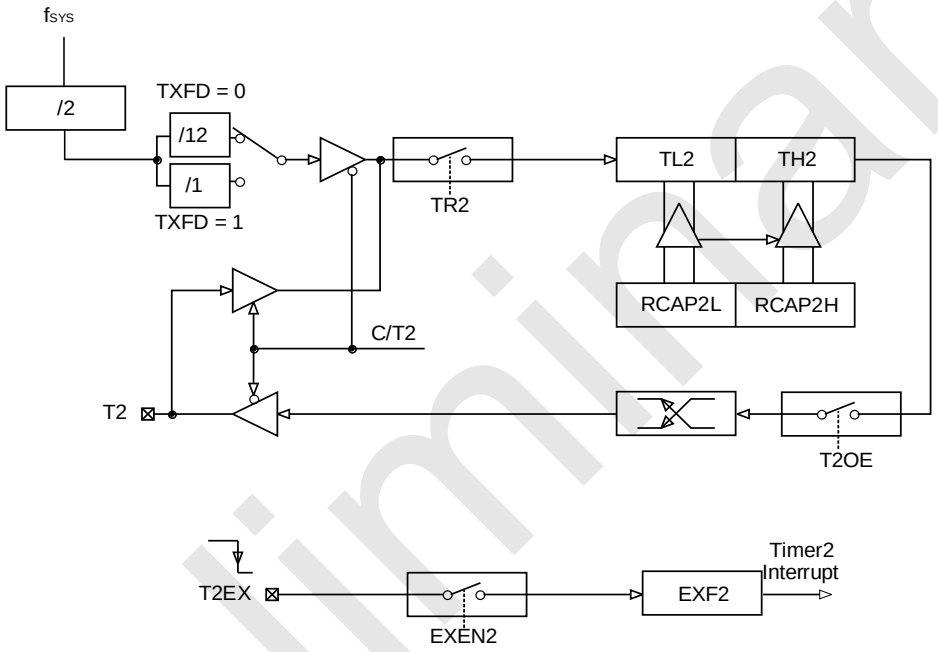
$$\text{Clock Out Frequency} = \frac{\text{fn2}}{(65536-[\text{RCAP2H,RCAP2L}])\times 4}$$

Where fn2 is the clock frequency of Timer 2:

$$\text{fn2} = \frac{f_{SYS}}{12};\ \text{T2FD} = 0$$

$$\text{fn2} = f_{SYS};\ \text{T2FD} = 1$$

Timer 2 overflow does not generate an interrupt. The T2 pin outputs the clock signal.



Mode 3: Programmable clock output

Note:

1. Both TF2 and EXF2 can trigger interrupt requests for Timer 2, and share the same vector address.
2. TF2 and EXF2 can be set to 1 by software when the event occurs or at any time. Only software reset or hardware reset can clear them to 0.
3. When EA = 1 and ET2 = 1, setting TF2 or EXF2 to 1 triggers Timer 2 interrupt.
4. When Timer 2 functions as a baud rate generator, writing to TH2/TL2 or RCAP2H/RCAP2L affects baud rate accuracy and may cause communication errors.

12 Multiplier/Divider

The SC92F531X provides one 16-bit multiplier/divider, composed of the extended accumulator EXA0-EXA3, the extended B register EXB, and the operation control register OPERCON. The hardware multiplier/divider does not use CPU cycles; operations are hardware-executed. It runs tens of times faster than software implementations and can replace software for 16-bit×16-bit multiplication and 32-bit/16-bit division operations.

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
EXA0	E9H	Extended Accumulator 0	EXA [7:0]								00000000b
EXA1	EAH	Extended Accumulator 1	EXA [15:8]								00000000b
EXA2	EBH	Extended Accumulator 2	EXA [23:16]								00000000b
EXA3	ECH	Extended Accumulator 3	EXA [31:24]								00000000b
EXBL	EDH	Extended Register B Low	EXB [7:0]								00000000b
EXBH	EEH	Extended Register B High	EXB [15:8]								00000000b
OPERCON	EFH	Operation Control Register	OPERS	MD	-	-	-	-	CRCRST	CRCSTA	00xxxx00b

OPERCON (EFH) Operation Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	OPERS	MD	-	-	-	-	-	CHKSUMS
Read/Write	R/W	R/W	-	-	-	-	-	R/W
Power-On Initial Value	0	0	x	x	x	x	x	0

Bit Number	Bit Symbol	Description
7	**OPERS**	Multiply/Divide unit operation start trigger control Write "1" to this bit to start a multiply/divide operation. This bit serves only as a trigger signal to start computation. When this bit is zero, it indicates the operation is complete. Only writing a value of 1 is valid for this bit
6	**MD**	Multiplier-Divider selection 0: Multiplication operation. Write the multiplicand and multiplier as follows, and read the product as shown:

Byte / Operand	Byte 3	Byte 2	Byte 1	Byte 0
Multiplicand 16-bit	-	-	EXA1	EXA0
Multiplier 16-bit	-	-	EXBH	EXBL
Product 32-bit	EXA3	EXA2	EXA1	EXA0

1: Division operation. Write the dividend and divisor as follows, and read the quotient and remainder:

Byte / Operand	Byte 3	Byte 2	Byte 1	Byte 0
Dividend 32-bit	EXA3	EXA2	EXA1	EXA0
Divisor 16-bit	-	-	EXBH	EXBL
Quotient 32-bit	EXA3	EXA2	EXA1	EXA0
Remainder 16-bit	-	-	EXBH	EXBL

Note:

1. During arithmetic operations, reading from or writing to EXA and EXB is prohibited.

2. The time required for multiplier/divider operation completion is 16/f_{SYS}.

13 General Pulse Width Modulation Counter PWM2

The SC92F531X provides 10 PWM channels, divided into two categories:

1. Multifunction PWM: a total of 8 channels grouped as PWM0, with output signal ports PWM00-07
2. General PWM: a total of 2 channels grouped as PWM2, with output signals PWM20-PWM21, where PWM21 is multiplexed on all I/O ports. See Port mapped register (R/W) .

Note: The period register of PWM2 shares Timer2's TL2 and TH2 registers. When using PWM2, do not modify Timer2's timing/counter values, as this may cause abnormal PWM period output.

13.1 PWM2 related registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
T2CON	C8H	Timer 2 Control Register	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000b
T2MOD	C9H	Timer 2 Working Mode register	T2FD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN	0x000000b
RCAP2L	CAH	Timer 2 Reload/Capture Low Byte	RCAP2L[7:0]								00000000b
RCAP2H	CBH	Timer 2 Reload/Capture High Byte	RCAP2H[7:0]								00000000b
TL2	CCH	Timer 2 Low Byte	TL2[7:0]								00000000b
TH2	CDH	Timer 2 High Byte	TH2[7:0]								00000000b

The following explains each register:

T2CON (C8H) Timer 2 control register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
2	**TR2**	Timer2 start/stop control bit 0: Stop Timer2 and stop the PWM2 counter 1: Start Timer2 and start the PWM2 counter

Timer2 can enter PWM mode when EPWM20 or EPWM21 is set to 1. At this time, T2 and T2EX are invalid, and PWM20 and PWM21 can output PWM waveforms.

T2MOD (C9H) Timer 2 working mode register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	T2FD	-	EPWM21	EPWM20	INV21	INV20	T2OE	DCEN
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
5	**ENPWM21**	PWM21 waveform output selection

Bit Number	Bit Symbol	Description
		0: PWM21 output is disabled 1: The I/O pin where PWM21 is located serves as the PWM waveform output port
4	**ENPWM20**	PWM20 waveform output selection 0: PWM20 output is disabled 1: The I/O pin where PWM20 is located serves as the PWM waveform output port
3	**INV21**	PWM21 waveform output inversion control 1: PWM21 waveform output is inverted 0: PWM21 waveform output is not inverted
2	**INV20**	PWM20 waveform output inversion control 1: PWM20 waveform output is inverted 0: PWM20 waveform output is not inverted

The TH2 and TL2 counters count up from 0. When the count matches the duty cycle setting PDTxy [15:0], the PWM output changes state, then the counters continue counting up to the auto-reload value PWMPDX, reset to 0, and generate an overflow event to complete one PWM cycle. If the timer interrupt is enabled, a timer interrupt will be triggered at this moment.

The calculation formula for the Timer output PWM period T_{PWM} is as follows:

$$T_{PWM} = \frac{PWMPDX[15:0] + 1}{f_{SYS}}$$

Duty cycle calculation formula:

$$duty = \frac{PDTxy\ [15:0]}{PWMPDX[15:0] + 1}$$

The PWM period is configured via the following registers:

RCAP2H (CBH) PWMn period register high byte (R/W)

Note: The PWM2 period register shares resources with Timer2. When using PWM2, do not modify Timer2's timing/counter values, as this may cause abnormal PWM period output.

Bit Number	7	6	5	4	3	2	1	0
Symbol	PWMPDH2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

RCAP2L (CAH) PWMn period register low byte (R/W)

Note: The PWM2 period register shares resources with Timer2. When using PWM2, do not modify Timer2's timing/counter values, as this may cause abnormal PWM period output.

Bit Number	7	6	5	4	3	2	1	0
Symbol	PWMPDL2[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**PWMPDX[15:0]**	PWMn period configuration This value represents (period – 1) of the PWM output waveform. In other words, the period value of the PWM output is equal to $(PWMPDX[15:0] + 1)/f_{SYS}$

PWM duty cycle is configured via the following registers:

PWM2 Duty Cycle Adjustment Register (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
118H	PDT20[15:8]								00000000b
119H	PDT20[7:0]								00000000b
11AH	PDT21[15:8]								00000000b
11BH	PDT21[7:0]								00000000b

Bit Number	Bit Symbol	Description
7-0	**PDT20[15:0]**	PWM20 duty cycle setting High-level width of PWM20's waveform: (PDT20[15:0]) / f_{SYS}
7-0	**PDT21[15:0]**	PWM21 duty cycle setting High-level width of PWM21's waveform: (PDT21[15:0]) / f_{SYS}

13.2 PWM2 duty cycle variation characteristics

To change the duty cycle of the PWM2 output waveform, adjust the value of the high-level setting register PDTx (x=0-1). Note: Changing the PDTx value will not immediately affect the duty cycle the update takes effect starting from the next cycle.

13.3 PWM2 period variation characteristics

When the PWM2 output waveform is active, if the period needs to be changed, this can be done by modifying the values of the period-setting registers TL2 and TH2. Changing these period register values causes the PWM output period to vary as follows:

Define the current period count as Tn, the timer count at the moment the period register is written as Tm, and the updated period count value as Tx. Then:

If Tm ≤ Tx: The period updates immediately to Tx

If Tm > Tx: The period update occurs in two phases. In the first phase, after writing to the period registers, the period counter continues counting from the current count until overflow and reset. In the second phase, the period changes to Tx.

14 Multifunction Pulse Width Modulation Counter PWM0

SC92F531X provides up to 10 PWM channels, divided into two categories:

1. Multifunction PWM: a total of 8 channels grouped as PWM0, with output signal ports PWM00-07
2. Regular PWM: 2 channels (PWM2), with output ports: PWM20-PWM21.

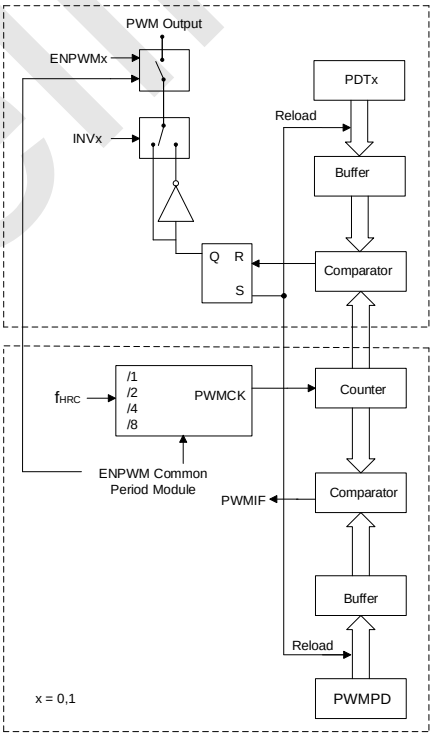
Note: The period register of PWM2 shares Timer2's TL2 and TH2 registers. When using PWM2, do not modify Timer2's timing/counter values, as this may cause abnormal PWM period output.

The multifunction PWM0 characteristics of the SC92F531X are as follows:

1. 16-bit PWM resolution
2. Output waveform can be inverted
3. Type: can be set as center-aligned or edge-aligned
4. Mode: can be set as independent mode or complementary mode
5. In independent mode, the 8 PWM channels share the same period, but the duty cycle of each PWM output waveform can be set individually
6. In complementary mode, four pairs of complementary pwm waveforms with dead time can be output simultaneously
7. Provides a pwm overflow interrupt
8. Supports a fault detection mechanism

PWM0 of the SC92F531X supports adjustment of period and duty cycle. The PWMCFG, PWMCON0, and PWMCON1 registers control the PWM status and period, while the enable state and duty cycle of each PWM channel's output can be adjusted individually.

14.1 PWM0 block diagram



SC92F531X PWM block diagram

14.2 PWM0 general configuration register

14.2.1 PWM0 general configuration register

Users can set the SC92F531X's PWM0 output mode to independent mode or complementary mode by setting PWMMD[1:0]. In independent mode, all eight PWM channels share the same period, but the duty cycle of each PWM output can be set independently. In complementary mode, four pairs of complementary PWM waveforms with dead time can be output simultaneously.

The PWM types of SC92F531X are divided into edge-aligned and center-aligned:

14.2.1.1 Edge-aligned:

The PWM counter counts up from 0. When the count matches the duty cycle setting PDTx[15:0], the PWM output switches state. The counter then continues counting up until it matches the period setting PWMPD[15:0] + 1, marking the end of one PWM period. The counter resets to zero thereafter. If the PWM interrupt is enabled, an interrupt will be generated at this point. The PWM output waveform is leading-edge aligned.

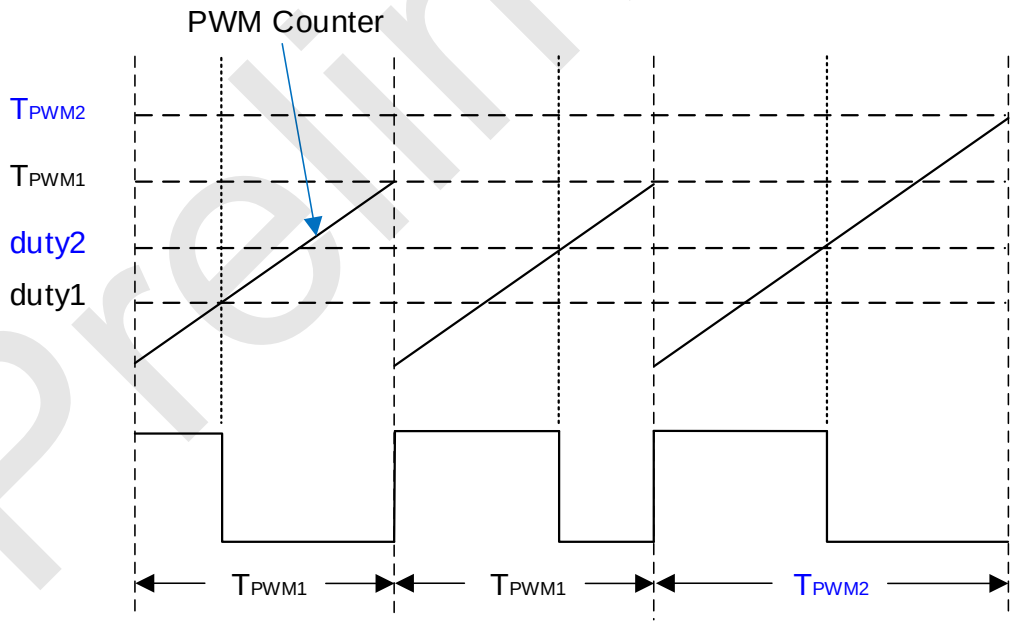
Edge-aligned type period T_{PWM} Calculation formula:

$$T_{PWM} = \frac{PWMPD[15:0] + 1}{f_{PWMCK}}$$

Edge-aligned type duty cycle calculation formula:

$$duty = \frac{PDTx\ [15:0]}{PWMPD[15:0] + 1}$$

The edge-aligned waveform diagram is shown below:



Edge-aligned PWM

14.2.1.2 Center-aligned type:

The PWM counter starts counting up from 0. When the count value matches the duty cycle setting PDTx[15:0], the PWM output changes state. The counter then continues counting up until it matches the period setting PWMPD[15:0] + 1 (the midpoint of the PWM period), at which point it automatically begins counting down. When the count matches PDTx[15:0] again, the PWM output changes state once more. The counter then counts down

to 0 (underflow), marking the end of one PWM period. If the PWM interrupt is enabled, a PWM interrupt will be triggered at this point.

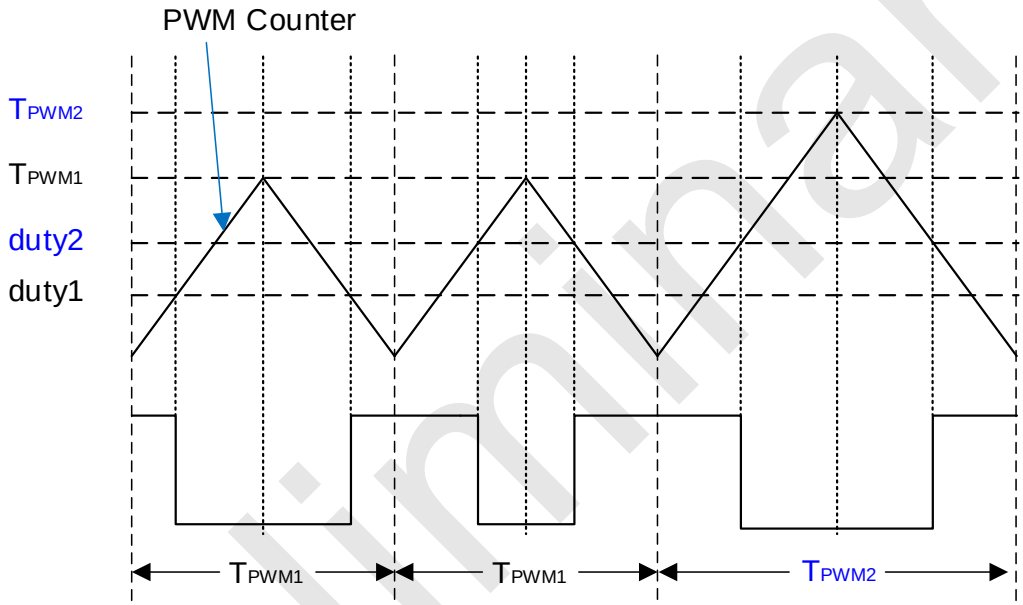
Center-aligned period T_{PWM} calculation formula:

$$Tpwm = 2 * \frac{PWMPD[15:0] + 1}{f_{PWMCK}}$$

Center-aligned duty cycle calculation formula:

$$duty = \frac{PDTx\ [15:0]}{PWMPD[15:0] + 1}$$

The center-aligned waveform diagram is as follows:



Center-aligned PWM

The above modes and types can be configured via the PWMCON0 register:

PWMCON0 (D2H) PWM0 control register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ENPWM	PWMIF	PWMCK[1:0]		-	-	PWMMD[1:0]	
Read/Write	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Power-On Initial Value	0	0	0	0	x	x	0	0

Bit Number	Bit Symbol	Description
7	**ENPWM**	PWM0 module enable control 1: Enable Clock to enter the PWM0 unit. PWM0 is in operational state. PWM0 output port status is controlled by the ENPWMx register (x=0-7) 0: PWM0 unit stops working. PWM0 counter is cleared. All PWM0 output ports are set to GPIO mode
6	**PWMIF**	PWM0 interrupt request flag When the PWM0 counter overflows (i.e., counts beyond PWMPD), this bit is automatically set to 1 by hardware. If IE1[1] (EPWM) is also set to 1 at this time, a PWM0 Interrupt is generated. After the PWM0

Bit Number	Bit Symbol	Description
		Interrupt occurs, this bit is not automatically cleared by hardware and must be cleared by software.
5-4	**PWMCK[1:0]**	PWM0 Clock Source Selector 00:f_{HRC} 01:f_{HRC}/2 10:f_{HRC}/4 11:f_{HRC}/8 f_{HRC} definition is as follows: High-frequency system clock circuit
1-0	**PWMMD[1:0]**	PWM0 operating mode configuration 0x: independent mode 1x: complementary mode x0: edge-aligned mode x1: center-aligned mode
3-2	**-**	Reserved

PWMCFG (D1H) PWM0 Configuration Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**INVx (x=0-7)**	PWM0x Waveform Output Inversion Control 1: PWM0x Waveform Output Inverted 0: PWM0x Waveform Output Not Inverted

PWMCON1 (D3H) PWM0 Control Register 1 (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EPWM7	EPWM6	EPWM5	EPWM4	EPWM3	EPWM2	EPWM1	EPWM0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**ENPWMx (x=0-7)**	PWM0x Waveform Output Selection 0: PWM0x Output Disabled and Used as a GPIO Port 1: When ENPWM=1, the PWM0x I/O Serves as Waveform Output Port

Note: If ENPWM is set to 1, the PWM0 module is enabled. However, if ENPWMx=0, the PWM0 output is disabled and used as a GPIO port. In this mode, the PWM0 module can be used as a 16-bit Timer. When EPWM (IE1.1) is set to 1, PWM0 will generate an interrupt.

PWMPDL (D4H) Period Register Low 8 bits (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	PWMPDL[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

PWMPDH (D5H) Period Register High 8 bits (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	PWMPDH[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**PWMPD[15:0]**	PWM0 shared period setting This value represents the PWM0 output waveform's (period – 1). That is, the PWM0 output period value equals to (PWMPD[15:0] + 1) / f_{PWMCK}

IE1 (A9H) Interrupt Enable Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	-	ECMP	-	-	EBTM	EPWM	ESSI
Read/Write	-	-	R/W	-	-	R/W	R/W	R/W
Power-On Initial Value	x	x	0	x	x	0	0	0

Bit Number	Bit Symbol	Description
1	**EPWM**	PWM0 interrupt enable control 0: Disable PWM0 Interrupt 1: Enable interrupt generation when PWM0 counter overflows

IP1 (B9H) Interrupt Priority Control Register 1 (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	-	IPCMP	-	-	IPBTM	IPPWM	IPSSI
Read/Write	-	-	R/W	-	-	R/W	R/W	R/W
Power-On Initial Value	x	x	0	x	x	0	0	0

Bit Number	Bit Symbol	Description
1	**IPPWM**	PWM0 interrupt priority selection 0: The interrupt priority of PWM0 is low 1: The interrupt priority of PWM0 is high

14.2.2 PWM0 Fault Detection Function Settings

Fault detection is commonly used for motor system protection. When fault detection is enabled by setting FLTEN1 (PWMFLT.7) to 1, the fault detection input pin (FLT) is activated. When the signal on the FLT pin meets the fault condition, the FLTSTA1 flag is set to 1 by hardware, PWM0 output stops, the PWM0 counter continues counting, and PWM0 interrupts remain unaffected. Fault detection modes include latch mode and immediate mode; In immediate mode, when the fault signal on the FLT pin meets the disable condition, the FLTSTA1 flag is cleared to 0 by hardware. The PWM0 counter continues counting until it reaches zero, after which PWM0 output resumes; In latch mode, when the fault signal at the FLT pin meets the disable condition, the FLTSTA1 flag bit status remains unchanged. The user can clear it by software. Once the FLTSTA1 status is cleared, the PWM0 counter continues counting down to zero, after which PWM0 output resumes.

PWMFLT (D7H) PWM Fault Detection Setting Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FLTEN1	FLTSTA1	FLTMD1	FLTLV1	-	-	FLTDT1[1:0]	

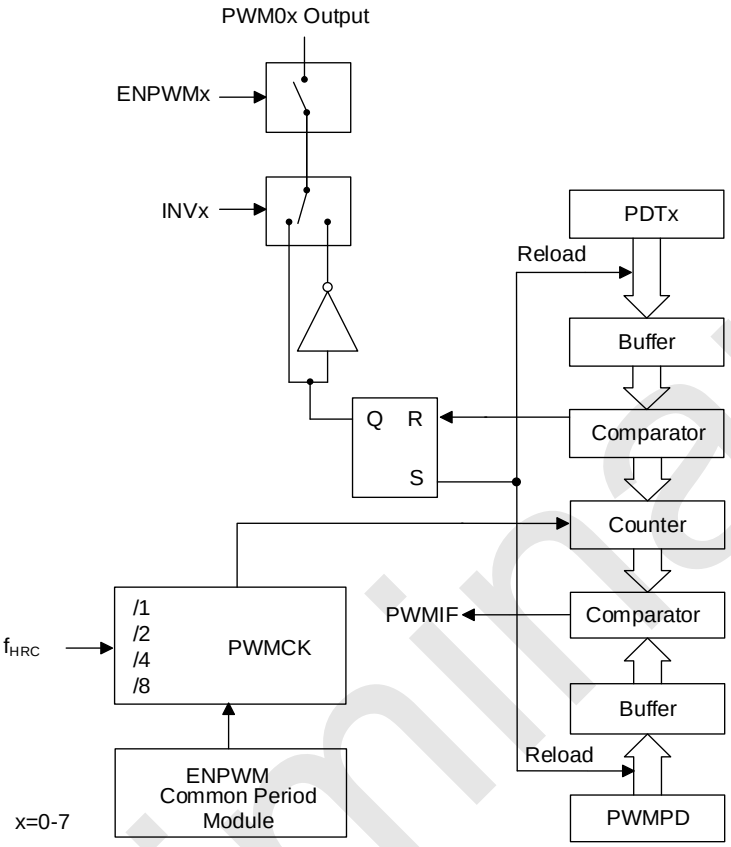
Bit Number	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	-	-	R/W	R/W
Power-On Initial Value	0	0	0	0	x	x	0	0

Bit Number	Bit Symbol	Description
7	**FLTEN1**	PWM0 Fault Detection Function Control Bit 0: Fault detection function off 1: Fault detection function on
6	**FLTSTA1**	PWM0 Fault Detection Status Flag Bit 0: PWM0 operates normally 1: Fault detection active PWM0 output is in a high-impedance state. If in latch mode, this bit can be cleared by software.
5	**FLTMD1**	PWM0 fault detection mode configuration bit 0: Latch mode. When fault input is active, FLTSTA1 is set to "1" and PWM0 output stops. When fault input is inactive, the FLTSTA1 status remains unchanged. 1: Immediate mode. When fault input is active, FLTSTA1 is set to "1" and PWM0 output stops. When fault input is inactive, FLTSTA1 is immediately cleared. The PWM0 waveform will resume output when the PWM0 time base counter resets to zero.
4	**FLTLV1**	PWM0 fault detection level select bit 0: Fault detection active low 1: Fault detection active high
1-0	**FLTDT1[1:0]**	PWM0 fault detection input signal filter time setting 00: Filter time set to 0 01: Filter time set to 1 μs 10: Filter time set to 4 μs 11: Filter time set to 16 μs
3-2	**-**	Reserved

14.3 Independent mode

In independent mode (PWMMD.1 = 0), the duty cycles of 8 PWM channels can be independently configured. The user first configures the PWM output state and period, then sets the duty cycle registers of the respective PWM channels to output PWM waveforms with fixed duty cycles.

14.3.1 PWM0 independent mode Block Diagram



SC92F531X PWM independent mode block diagram

14.3.2 PWM0 independent mode duty cycle configuration

PWM0 Duty Cycle Adjustment Register PDTx (R/W)

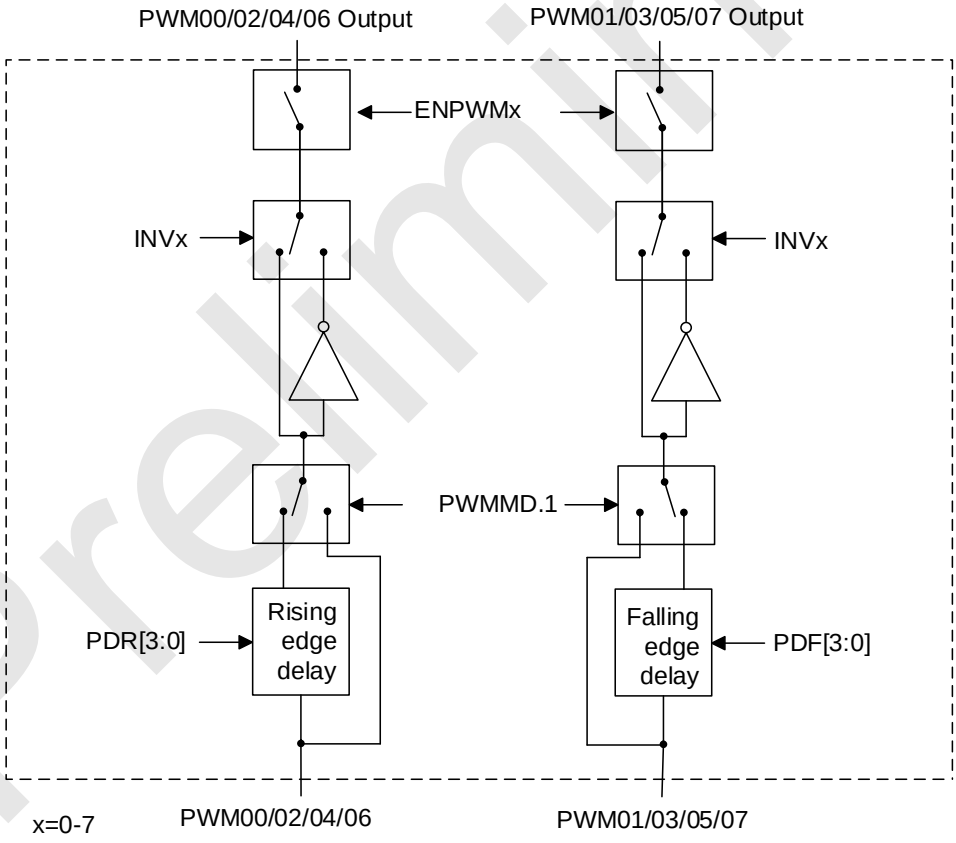
Address	7	6	5	4	3	2	1	0	Power-On Initial Value
108H	PDT00[15:8]								00000000b
109H	PDT00[7:0]								00000000b
10AH	PDT01[15:8]								00000000b
10BH	PDT01[7:0]								00000000b
10CH	PDT02[15:8]								00000000b
10DH	PDT02[7:0]								00000000b
10EH	PDT03[15:8]								00000000b
10FH	PDT03[7:0]								00000000b
110H	PDT04[15:8]								00000000b
111H	PDT04[7:0]								00000000b
112H	PDT05[15:8]								00000000b
113H	PDT05[7:0]								00000000b

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
114H	PDT06[15:8]								00000000b
115H	PDT06[7:0]								00000000b
116H	PDT07[15:8]								00000000b
117H	PDT07[7:0]								00000000b

Bit Number	Bit Symbol	Description
15-0	**PDTx [15:0] (x=0-7)**	PWM0x Waveform Duty Cycle Length Setting The high-level width of the PWM0x waveform is equal to (PDTx [15:0]* / f_{PWMCK}).

14.4 Complementary Mode

14.4.1 PWM0 Complementary Mode Block Diagram



SC92F531X PWM Complementary Mode Block Diagram

14.4.2 PWM0 complementary mode duty cycle configuration

In complementary mode (PWMMD[1:0] = 1x), PWM00/PWM01, PWM02/PWM03, PWM04/PWM05, and PWM06/PWM07 are divided into four groups, and their duty cycles are respectively adjusted via PDT0[15:0], PDT2[15:0], PDT4[15:0], and PDT6[15:0].

In complementary mode, registers PDT1[15:0], PDT3[15:0], PDT5[15:0], and PDT7[15:0] are invalid.

PWM0 Duty Cycle Adjustment Register PDTx (R/W)

Address	7	6	5	4	3	2	1	0	Power-On Initial Value
108H	PDT00[15:8]								00000000b
109H	PDT00[7:0]								00000000b
10AH	PDT01[15:8]								00000000b
10BH	PDT01[7:0]								00000000b
10CH	PDT02[15:8]								00000000b
10DH	PDT02[7:0]								00000000b
10EH	PDT03[15:8]								00000000b
10FH	PDT03[7:0]								00000000b
110H	PDT04[15:8]								00000000b
111H	PDT04[7:0]								00000000b
112H	PDT05[15:8]								00000000b
113H	PDT05[7:0]								00000000b
114H	PDT06[15:8]								00000000b
115H	PDT06[7:0]								00000000b
116H	PDT07[15:8]								00000000b
117H	PDT07[7:0]								00000000b

Bit Number	Bit Symbol	Description
15-0	**PDTx [15:0] (x=0,2,4,6)**	Duty cycle length settings for PWMx and PWMy waveforms (y = x + 1) The high-level pulse width of the PWM waveform on pins Px and Py is (PDTx [15:0] / f_{PWMCK})

14.4.3 PWM0 complementary mode dead time settings

When PWM0 of the SC92F531X operates in complementary mode, the dead zone control module prevents overlap between the two complementary PWM output signals, ensuring that the pair of complementary power switches driven by the PWM signals do not conduct simultaneously.

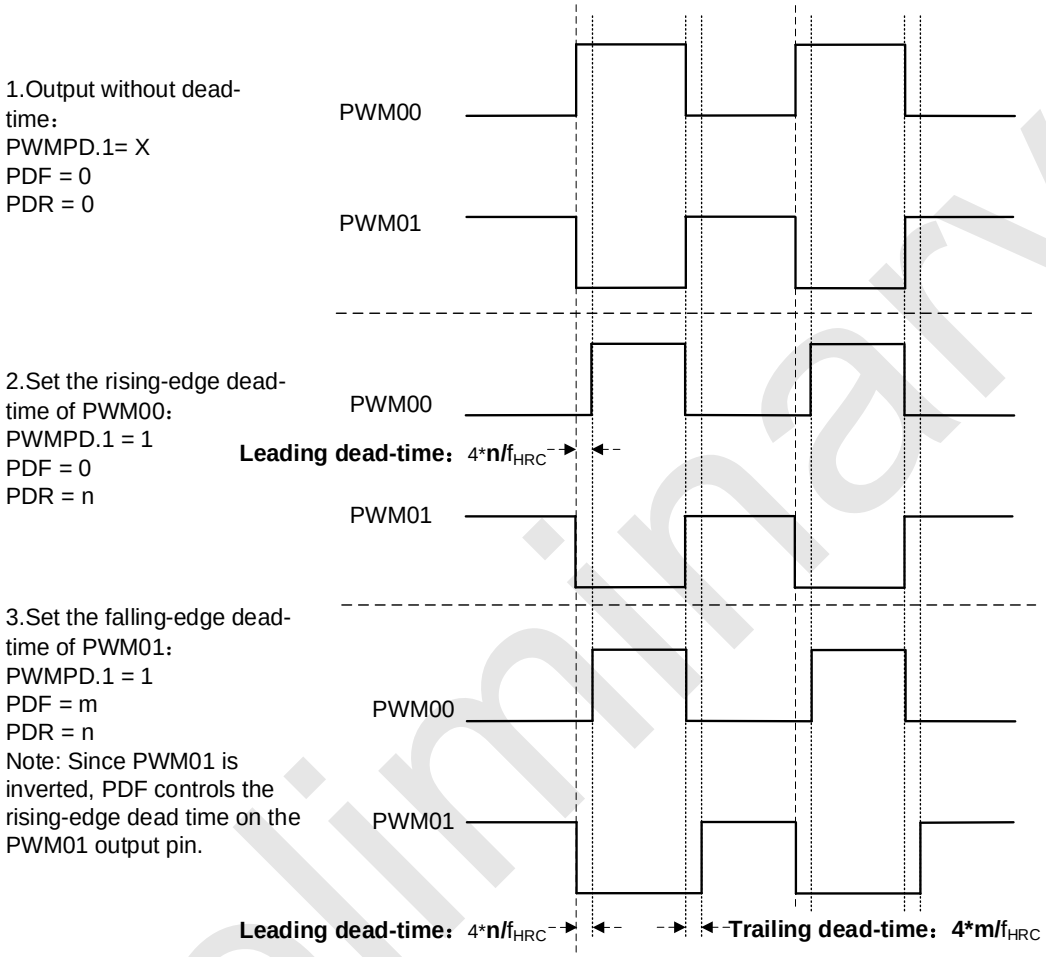
PWMDFR (D6H) PWM0 Dead Time Setting Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	**PDF[3:0]**				**PDR[3:0]**			
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-4	**PDF[3:0]**	Complementary mode: PWM falling edge dead time = 4*PDF[3:0] / f_{HRC}
3-0	**PDR[3:0]**	Complementary mode: PWM rising edge dead time = 4*PDR[3:0] / f_{HRC}

14.4.4 PWM dead time output waveform

The figure below illustrates the dead time adjustment waveforms of PWM00 and PWM01 in complementary mode. For clarity, PWM01 is shown inverted (INV1=1).



PWM dead time output waveform

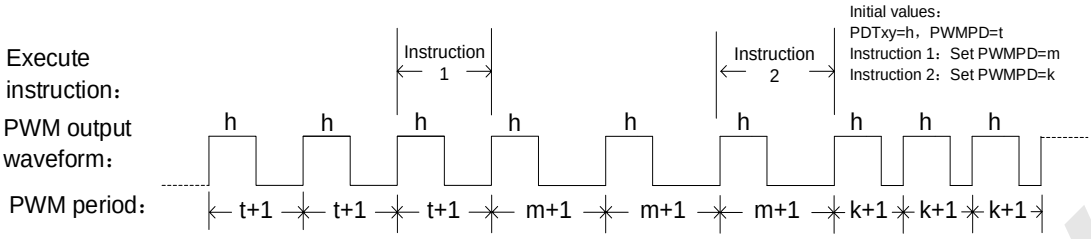
14.5 PWM0 waveform and applications

The effects of various SFR parameter changes on the PWM0 waveform are described below:

1. Duty cycle update behavior

When outputting PWMn waveforms, changing the duty cycle can be done by modifying the value of the high-level setting register (PDTx). Note: Changing the PDTx value does not immediately affect the duty cycle; the change takes effect at the start of the next cycle.

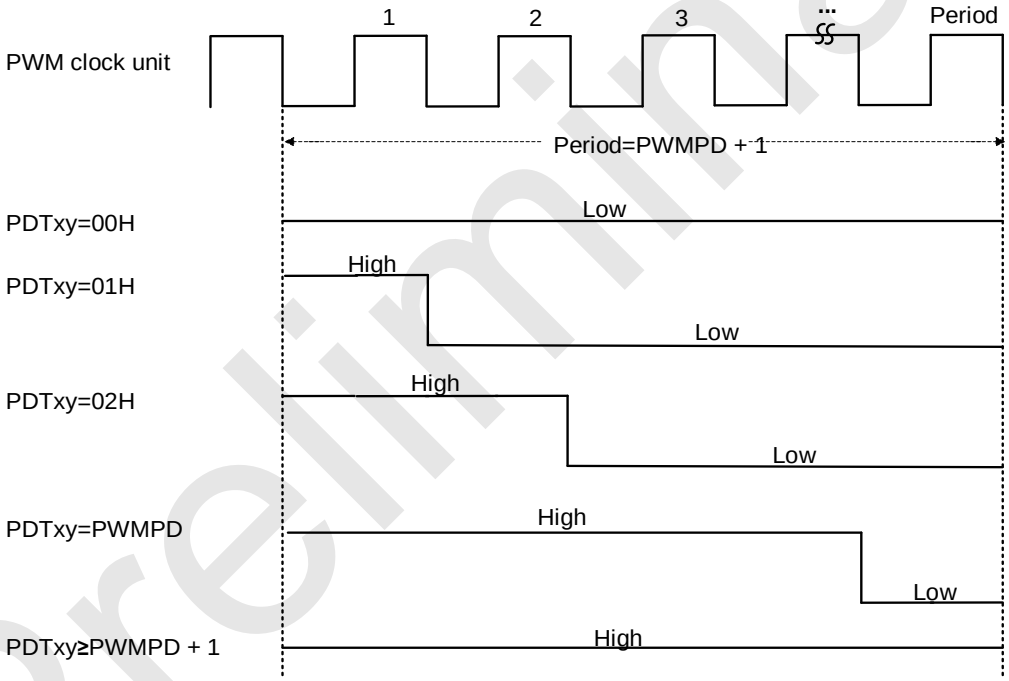
2. Period update behavior



Period update behavior diagram

When outputting PWM0 waveforms, changing the period can be done by modifying the value of the period setting register PWMPD. Changing the PWMPD value does not immediately alter the period; the change takes effect after the current period ends, applying from the next period onward, as shown in the diagram above.

3. Relationship between period and duty cycle



The relationship between period and duty cycle

The relationship between the period and duty cycle is shown in the figure above. This result assumes that PWM0 output inversion control (INV0x, x=0-7) is initially set to 0. To achieve the opposite result, set INV0x to 1.

15 GP I/O

The SC92F531X provides 22 controllable bidirectional GPIO ports. The input/output control registers control each port's input and output states. When configured as an input, each IO port includes an internal pull-up resistor controlled by PxPHy. These 22 IO ports are multiplexed with other functions. When the IO port is in input or output mode, the actual status value of the port is read from the port data register.

Note: Unused and packaged IO ports that are not exposed must be set to strong push-pull output mode.

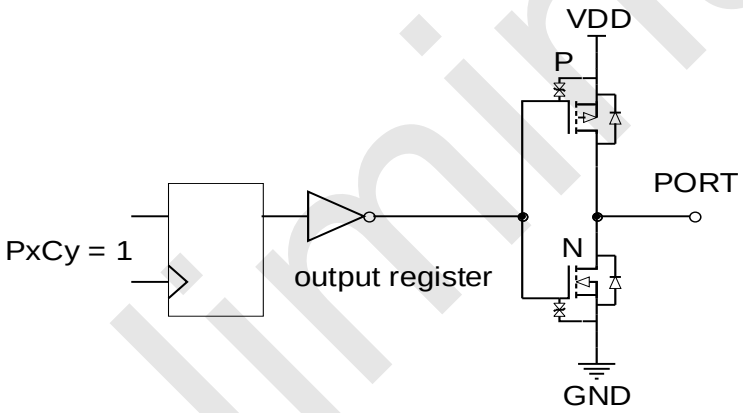
15.1 GPIO schematic diagram

15.1.1 Strong push-pull output mode

In strong push-pull output mode, continuous high-current drive can be provided:

- Ports P0 and P1 support 22 mA @ 4.3 V for high-level output and 80 mA @ 0.8 V for low-level output
- Port P2 supports 22 mA @ 4.3 V for high-level output and 130 mA @ 0.8V for low-level output

The schematic diagram of the port structure in strong push-pull output mode is as follows:

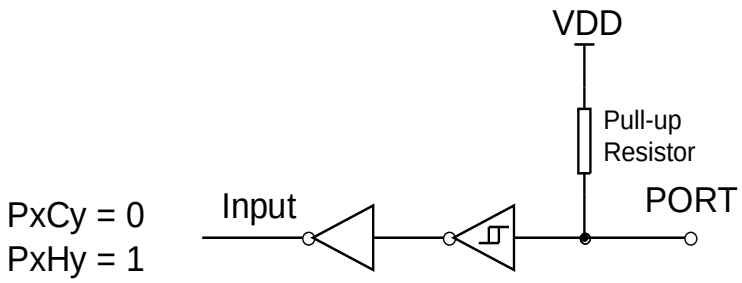


Strong push-pull output mode

15.1.2 Input mode with pull-up resistor

In input mode with a pull-up resistor, the input pin is continuously connected to a pull-up resistor, and a low-level signal is detected only when the input pin voltage is pulled low.

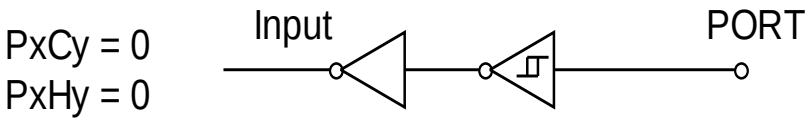
The schematic diagram of the port structure in input mode with pull-up resistor is as follows:



Input mode with pull-up resistor

15.1.3 High-impedance input mode (Input only)

The schematic of the port structure in high-impedance input mode is shown below:



High-impedance input mode

15.2 I/O port related registers

P0CON (9AH) P0 port Input/Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P0C7	P0C6	P0C5	P0C4	P0C3	P0C2	P0C1	P0C0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P0PH (9BH) P0 port Pull-up Resistor Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P0H7	P0H6	P0H5	P0H4	P0H3	P0H2	P0H1	P0H0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P1CON (91H) P1 port Input/Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	P1C5	P1C4	P1C3	P1C2	P1C1	P1C0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

P1PH (92H) P1 port Pull-up Resistor Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	P1H5	P1H4	P1H3	P1H2	P1H1	P1H0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

P2CON (A1H) P2 port Input/Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P2C7	P2C6	P2C5	P2C4	P2C3	P2C2	P2C1	P2C0

Bit Number	7	6	5	4	3	2	1	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P2PH (A2H) P2 port Pull-up Resistor Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P2H7	P2H6	P2H5	P2H4	P2H3	P2H2	P2H1	P2H0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**PxCy (x=0,2,y=0-7; x=1,y=0-5)**	Px Port Input/Output Control: 0: Pxy is Input Mode (Power-On Default) 1: Pxy is Push-Pull Output Mode
7-0	**PxHy (x=0,2,y=0-7; x=1,y=0-5)**	Px Port Pull-Up Resistor Setting (Valid only when PxCy=0): 0: Pxy is High-Impedance Input Mode (Power-On Default), Pull-Up Resistor Disabled 1: Pxy Pull-Up Resistor Enabled

P0 (80H) P0 Port Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

P1 (90H) P1 Port Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

P2 (A0H) P2 Port Data Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**P0.x (x=0-7)**	P0 Port Latch Register Data
5-0	**P1.x (x=0-5)**	P1 Port Latch Register Data
7-0	**P2.x (x=0-7)**	P2 Port Latch Register Data

16 Independent full-duplex UART serial communication port

The SC92F531X supports an independent full-duplex UART serial port, which can be conveniently used for connections with other devices or equipment, such as WiFi module circuits or other UART communication interface driver chips.

The functions and features of UART0 are as follows:

- Three communication modes are available: mode 0, mode 1, and mode 3
- Timer 1 or Timer 2 can be selected as the baud rate generator
- Completion of transmission and reception can generate Interrupts RI/TI. These interrupt flags must be cleared by software by writing 0 to RI/TI.
- UART0 pins TXD0 and RXD0 can be multiplexed on any pins. For details, see Port mapped register (R/ W).

16.1 UART0 Register

SCON (98H) Serial Port Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-6	**SM0-1**	Serial communication mode control bits 00: Mode 0, 8-bit half-duplex synchronous communication mode, with serial data transmitted and received on the RXD0 pin. The TXD0 pin serves as the transmit shift clock. Each frame transmits and receives 8 bits, least significant bit first 01: Mode 1, 10-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, and 1 stop bit. The communication baud rate is variable 10: Reserved 11: Mode 3, 11-bit full-duplex asynchronous communication, consisting of 1 start bit, 8 data bits, 1 programmable 9th bit, and 1 stop bit. The communication baud rate is variable.
5	**SM2**	Serial communication mode control bit 2 this bit is only valid in mode 3 0: RI is set to generate an Interrupt Request for each complete data frame received 1: RI is set to generate an interrupt request upon receiving a complete data frame only if RB8=1.
4	**REN**	Receive enable control bit 0: Receiving data is disabled 1: Receiving data is enabled.
3	**TB8**	Valid only in mode 3 corresponds to the 9th bit of transmitted data
2	**RB8**	Valid only in mode 3 corresponds to the 9th bit of received data
1	**TI**	Transmit interrupt flag bit set to 1 by hardware after transmission completes and must be cleared by user software writing 0
0	**RI**	Receive interrupt flag bit set to 1 by hardware after reception completes and must be cleared by user software writing 0

SBUF (99H) Serial port data buffer Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SBUF[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**SBUF[7:0]**	Serial port data buffer register SBUF includes two registers: a transmit shift register and a receive latch. Writing to SBUF loads data into the transmit shift register and starts the transmission process, while reading from SBUF returns the data stored in the receive latch.

PCON (87H) Power supply management control Register (W, *not readable*)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SMOD	-	-	-	RST	-	STOP	IDL
Read/Write	W	-	-	-	W	-	W	W
Power-On Initial Value	0	x	x	x	n	x	0	0

Bit Number	Bit Symbol	Description
7	**SMOD**	● When SM0-1 = 01 (UART0 mode 1) or SM0-1 = 11 (UART0 mode 3), the baud rate multiplier bit is set as follows: ■ 0: Serial port operates with the system clock divided by 1 ■ 1: Serial port operates with the system clock divided by 16 ● When SM0-1 = 00 (UART0 mode 0) baud rate multiplier bit: ■ 0: The serial port operates at system clock divided by 12 ■ 1: The serial port operates at system clock divided by 4

16.2 UART0 communication baud rate

In mode 0, the baud rate can be programmed as system clock divided by 12 or 4, decided by the SMOD (PCON.7) bit. When SMOD is 0, the serial port operates at system clock divided by 12. When SMOD is 1, the serial port operates at system clock divided by 4.

In modes 1 and 3, the serial port clock source can be programmed as system clock divided by 1 or 16, decided by the SMOD (PCON.7) bit. When SMOD is 0, the serial port operates at system clock divided by 1. When SMOD is 1, the serial port operates with the system clock divided by 16. Once the serial port clock source is determined, the baud rate overflow is configured via Timer 1 or Timer 2:

- When both TCLK (TXCON.4) and RCLK (TXCON.5) bits are 0, Timer 1 operates in baud rate generator mode, and the baud rate overflow for UART0 is set by [TH1, TL1]. The formula is as follows note: when Timer 1 is used as the baud rate generator, Timer 1 must stop counting, i.e., TR1=0:
  - SMOD = 0: $\mathrm{BaudRate} = \frac{f_{SYS}}{[TH1,TL1]}$ (Note: [TH1, TL1] must be greater than 0x0010
  - SMOD = 1: $\mathrm{BaudRate} = \frac{1}{16} * \frac{f_{SYS}}{[TH1,TL1]}$

- When either TCLK (TXCON.4) or RCLK (TXCON.5) is set to 1, Timer 2 operates in baud rate generator mode, and the UART0 baud rate overflow value is determined by [RCAP2H, RCAP2L], as shown in the following formula:
  - SMOD = 0: $\text{BaudRate} = \frac{f_{SYS}}{[RCAP2H,RCAP2L]}$ (Note: [RCAP2H, RCAP2L] must be greater than 0x0010 **)**
  - SMOD = 1: $\text{BaudRate} = \frac{1}{16} * \frac{f_{SYS}}{[RCAP2H,RCAP2L]}$

17 Three-in one serial communication interface

The SC92F531X internally integrates a three-in-one serial communication interface which can be used as UART/SPI/TWI (SSI), enabling easy connection between the MCU and devices or equipment with different interfaces. Users can set the SSMOD[1:0] bits in the OTCON register to configure the SSI interface as one of SPI, TWI, or UART communication modes. The key features are as follows:

1. In SPI mode, the interface can be configured as either master or slave.
2. In TWI mode, communication is limited to slave operation only.
3. UART mode supports operation in mode 1 (10-bit full-duplex asynchronous communication) and mode 3 (11-bit full-duplex asynchronous communication).
4. SSI pins SSICK0, SSITX0, and SSIRX0 can be multiplexed on any pins. See Port mapped register (R/W).

The specific configuration method is as follows:

OTCON (8FH) Output Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SSMOD[1:0]		-	-	-	-	-	-
Read/Write	R/W	R/W	-	-	-	-	-	-
Power-On Initial Value	0	0	x	x	x	x	x	x

Bit Number	Bit Symbol	Description
7-6	**SSMOD[1:0]**	SSI communication mode control bits 00: SSI off 01: SSI set to SPI communication mode 10: SSI set to TWI communication mode 11: SSI set to UART communication mode

17.1 SPI

When SSMOD[1:0] = 01, the SSI three-choice serial interface is configured as SPI. Serial Peripheral Interface (SPI) is a high-speed serial communication interface that allows the MCU to perform full-duplex synchronous serial communication with peripheral devices (including other MCUs).

17.1.1 Registers related to SPI operation

SSCON0 (9DH) SPI control register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SPEN	-	MSTR	CPOL	CPHA	SPR2	SPR1	SPR0
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**SPEN**	SPI enable control 0: Disable SPI 1: Enable SPI
5	**MSTR**	SPI master/slave selection 0: SPI as slave device 1: SPI as master device

Bit Number	Bit Symbol	Description
4	**CPOL**	Clock polarity control bit 0: SCK is low in idle state 1: SCK is high in idle state
3	**CPHA**	Clock phase control bit 0: Data sampled on first edge of SCK cycle 1: Data sampled on second edge of SCK cycle
2-0	**SPR[2:0]**	SPI clock rate selection bit 000:f_{SYS} /4 001:f_{SYS} /8 010:f_{SYS} /16 011:f_{SYS} /32 100:f_{SYS} /64 101:f_{SYS} /128 110:f_{SYS} /256 111:f_{SYS} /512
6	**-**	Reserved

SSCON1 (9EH) SPI status register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SPIF	WCOL	-	-	TXE	DORD	-	TBIE
Read/Write	R/W	R/W	-	-	R/W	R/W	-	R/W
Power-On Initial Value	0	0	x	x	0	0	x	0

Bit Number	Bit Symbol	Description
7	**SPIF**	SPI data transfer flag bit 0: Cleared by software 1: Indicates data transmission is complete set to 1 by hardware
6	**WCOL**	Write conflict flag bit 0: Cleared by software to indicate the write conflict has been handled 1: Set by hardware to indicate a conflict was detected
3	**TXE**	Transmit buffer empty flag 0: Transmit buffer is not empty 1: Transmit buffer is empty must be cleared by software
2	**DORD**	Transfer direction select bit 0: MSB sent first 1: LSB sent first
0	**TBIE**	Transmit buffer interrupt enable control bit 0: Interrupt not generated when TXE=1 1: SPI interrupt generated when TXE=1
5-4，1	**-**	Reserved

SSDAT (9FH) SPI data register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SPD[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Number	7	6	5	4	3	2	1	0
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**SPD[7:0]**	SPI data buffer register Data written to SSDAT is loaded into the transmit shift register. Reading SSDAT retrieves data from the receive shift register.

17.1.2 Signal Description

Master Out Slave In (MOSI):

This signal connects the master device to a slave device. Data is serially transmitted via MOSI from the master device to the slave device, with the master as output and the slave as input.

Master In Slave Out (MISO):

This signal connects a slave device to the master device. Data is serially transmitted via MISO from the slave device to the master device, with the slave as output and the master as input. When SPI is configured as a slave and is not selected, the slave device's MISO pin is in a high-impedance state.

SPI Serial Clock (SCK):

The SCK signal synchronizes data input and output on the MOSI and MISO lines. One byte is transferred every 8 clock cycles. If the slave device is not selected, it ignores the SCK signal.

17.1.3 Operating mode

SPI can be configured to operate in either master mode or slave mode. The SPI module is configured and initialized by setting the SSCON0 register (SPI control register) and SSCON1 (SPI status register). After configuration, data transfer is carried out by setting SSCON0, SSCON1, and SSDAT (SPI data register).

During SPI communication, data is shifted in and out serially and synchronously. The Serial Clock line (SCK) synchronizes the movement and sampling of data on the two serial data lines (MOSI and MISO). If the slave device is not selected, it does not participate in activity on the SPI bus.

When the SPI master transmits data to the slave via the MOSI line, the slave simultaneously sends data back to the master through the MISO line, enabling synchronous full-duplex transmission under the same clock. The send shift register and the receive shift register share the same special function register address. Writing to the SPI data register SSDAT updates the send shift register, while reading from the SSDAT register retrieves data from the receive shift register.

Some devices' SPI interfaces include an SS pin (Slave Select pin, active low). When communicating with the SC92F531X via SPI, the connection method for the SS pins of other devices on the SPI bus must follow the requirements of different communication modes. The table below shows how to connect the SS pins of other devices on the SPI bus under different SC92F531X SPI communication modes:

SPI	Other devices on the SPI bus	Mode	Slave SS (Slave Select pin)
Master Mode	Slave Mode	Single Master Single Slave	Pull Low
		Single Master Multiple Slaves	The SC92F531X provides multiple I/O pins, each connected to the SS pin of a slave device. Before data transmission, the slave device's SS pin must be pulled low.
Slave Mode	Master Mode	Single Master Single Slave	Pull High

17.1.3.1 Master Mode

- **Mode Start**

The SPI master initiates all data transmissions on the SPI bus. When the MSTR bit in the SSCON0 register is set to 1, SPI operates in master mode, allowing only one master to initiate transmission.

- **Transmit**

In SPI master mode, writing a byte to the SPI data register SSDAT loads the data into the transmit shift buffer. If the transmit shift register already holds data, the SPI master generates a WCOL signal indicating a write collision due to a write operation occurring too quickly. However, the data in the transmit shift register is unaffected, and transmission will not be interrupted. Additionally, if the transmit shift register is not empty, the master device immediately shifts out data from the transmit shift register to the MOSI line serially, synchronized to the SPI clock frequency on SCK. When the transmission completes, the SPIF bit in the SSCON1 register is set to 1. If SPI interrupt is enabled, an interrupt will be generated when the SPIF bit is set.

- **Reception**

When the master device sends data to the slave device via the MOSI line, the slave simultaneously transmits the contents of its transmit shift register to the master's receive shift register via the MISO line, enabling full-duplex communication. Therefore, setting the SPIF flag bit to 1 indicates both the transfer and data reception are complete. Data received from the slave device is stored in the master's receive shift register following the MSB or LSB first transfer direction. Once a byte has been fully shifted into the receive register, the processor can read the data from the SSDAT register.

17.1.3.2 Slave Mode

- **Mode Start**

When the MSTR bit in the SSCON0 register is cleared to 0, SPI operates in slave mode.

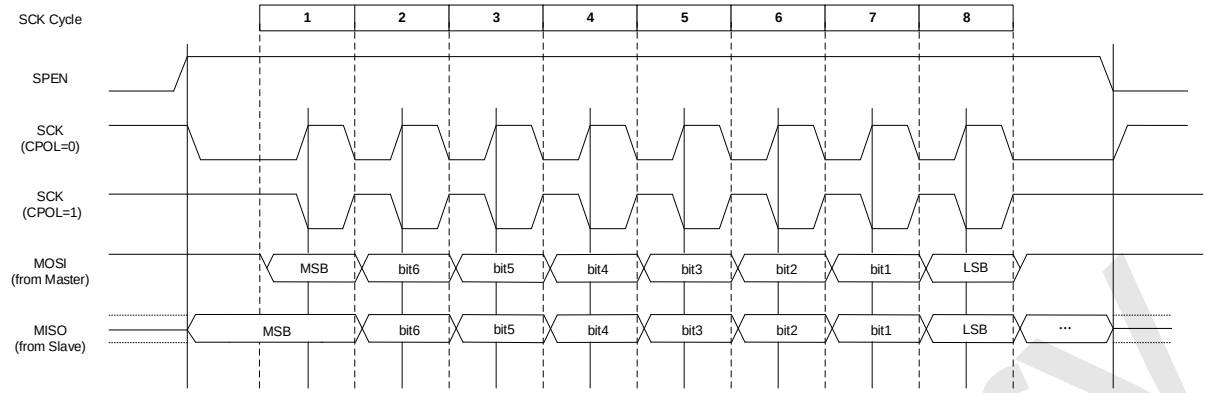
- **Transmission and reception:**

In slave mode, data is shifted in through the MOSI pin and shifted out through the MISO pin, synchronized with the SCK signal controlled by the master device. A bit counter tracks the number of SCK edges. When 8 bits (one byte) have been shifted into the receive shift register and simultaneously 8 bits (one byte) have been shifted out from the transmit shift register, the SPIF flag bit is set to 1. The data can then be read from the SSDAT register. If the SPI Interrupt is enabled, an interrupt will be generated when SPIF is set to 1. At this point, the receive shift register retains its current data and SPIF remains set to 1, preventing the SPI slave from receiving any new data until SPIF is cleared to 0. The SPI slave must write the data to be transmitted into the transmit shift register before the master starts a new data transfer. If no data is written before transmission begins, the slave will send a "0x00" byte to the master. If a write to SSDAT occurs during transmission, the SPI slave's WCOL flag is set. This indicates a write SSDAT collision when the transmit shift register already contains data. However, the shift register data remains unchanged and the transmission continues uninterrupted.

17.1.4 Transmission mode

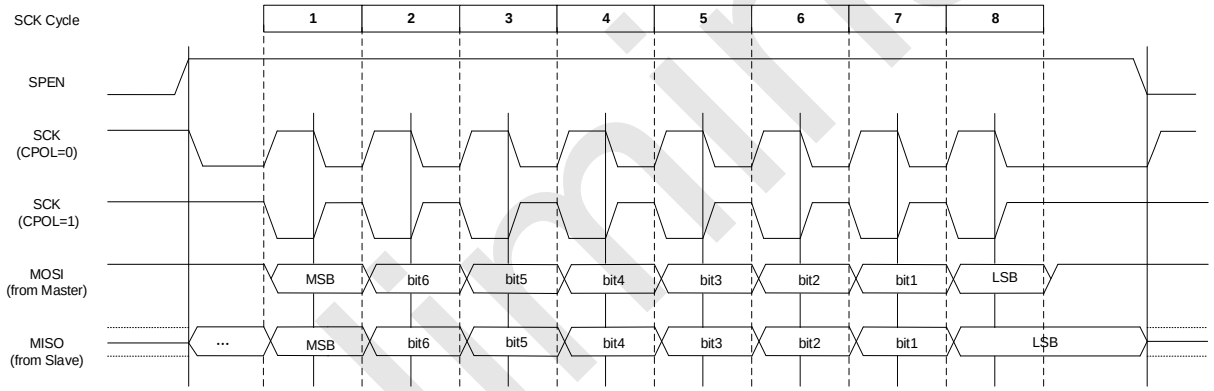
By setting the CPOL and CPHA bits in the SSCON0 register via software, users can select one of four combinations of SPI clock polarity and phase. The CPOL bit defines the polarity of the clock, i.e., the idle level state. It has minimal effect on the SPI transmission mode. The CPHA bit defines the clock phase, specifying which clock edge is used for data sampling and shifting. The clock polarity and phase settings must be consistent between the master and slave devices in communication.

When CPHA = 0, data is captured on the first SCK edge. The slave device must have data ready before this first edge.



CPHA = 0 data transmission diagram

When CPHA = 1, the master outputs data to the MOSI line on the first SCK edge. The slave uses this first edge as a start signal and begins capturing data on the second edge. Therefore, the user must complete writing to SSDAT within these first two SCK edges. This data transfer mode is the preferred communication method between one master device and one slave device.



CPHA = 1 Data Transfer Diagram

17.1.5 Error Detection

Writing to the SSDAT register during data sequence transmission causes a write conflict, setting the WCOL bit in the SSCON1 register to 1. The WCOL bit being set does not trigger an interrupt nor abort transmission. The WCOL bit must be cleared by software.

17.2 TWI

With SSMOD[1:0] = 10, the three-choice serial interface SSI is configured as a TWI interface. The SC92F531X can only operate as a slave in TWI communication.

SSCON0 (9DH) TWI Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	TWEN	TWIF	-	GCA	AA	STATE[2:0]		
Read/Write	R/W	R/W	-	Read	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	x	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**TWEN**	TWI enable control 0: Disable TWI

Bit Number	Bit Symbol	Description
		1: Enable TWI
6	**TWIF**	TWI interrupt flag 0: Cleared by software 1: The interrupt flag is set to 1 by hardware under the following conditions ①First frame address matched ②Successfully received or transmitted 8-bit data ③Restart ④Slave device received stop signal
4	**GCA**	General address response flag bit 0: No response to general address 1: When GC is set to 1, this bit is set by hardware upon a matching general address, and then automatically cleared
3	**AA**	Receive enable bit 0: Reception of host-sent messages not permitted 1: Reception of host-sent messages permitted
2-0	**STATE[2:0]**	State machine status flag bits 000: Slave is idle, waiting for TWEN = 1 and detecting TWI start signal. Transitions to this state after receiving a stop condition. 001: Slave receiving first frame address and R/W bit (bit 8: 1=read, 0=write). Enters this state after detecting a start condition. 010: Slave receiving data state 011: Slave sending data state 100: While in slave sending data state, transitions here when the master returns UACK (acknowledge bit high), waiting for restart or stop condition. 101: Slave waiting for restart or stop condition after clearing AA bit during data sending.
5	**-**	Reserved

SSCON1 (9EH) TWI Address Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TWA[6:0]							GC
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-1	**TWA[6:0]**	TWI address register
0	**GC**	TWI general address enable 0: Disable response to general address 1: Enable response to general address

SSDAT (9FH) TWI Data Buffer Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TWDAT[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**TWDAT[7:0]**	TWI data buffer register

17.2.1 Signal Description

17.2.1.1 TWI Clock Signal Line (SCL)

This clock signal is generated by the master and connected to all slaves. One byte of data is transmitted during every 9 clock cycles. The first 8 cycles are used to transmit data, and the ninth clock cycle is for the receiver's acknowledgment.

17.2.1.2 TWI Data Signal Line (SDA)

SDA is a bidirectional signal line and should remain high when idle. It is pulled up by a pull-up resistor on the SDA line.

17.2.2 Operating mode

The TWI communication on the SC92F531X supports slave mode only:

- **Mode start**

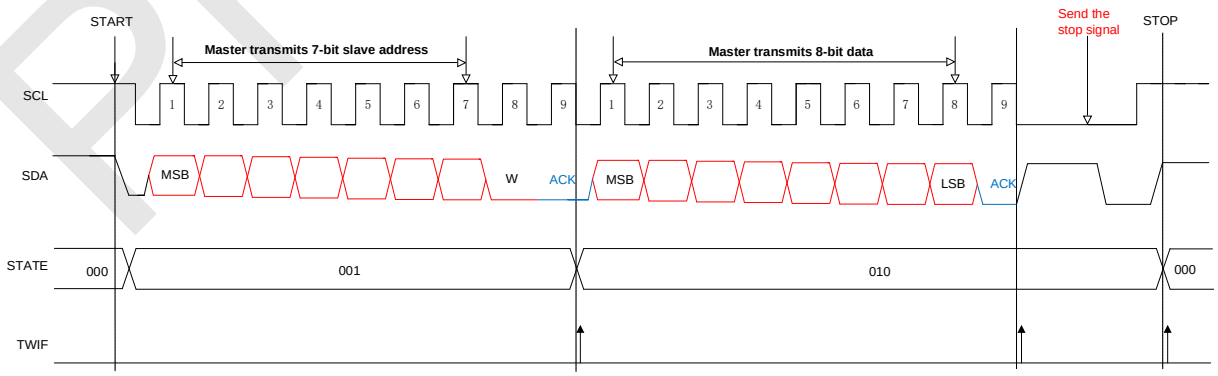
When the TWI enable flag (TWEN = 1) is set and a start signal is received from the master, the mode starts.

The slave switches from idle mode (STATE[2:0] = 000) to the state of receiving the first frame address (STATE[2:0] = 001), waiting for the master's first frame data. The first frame sent by the master consists of a 7-bit address and a 1-bit read/write bit. All slaves on the TWI bus receive this first frame. After sending the first frame, the master releases the SDA line. If the address sent by the master matches the value in the slave's own address register, that slave is selected. The selected slave then examines the 8th bit on the bus, which is the data read/write bit (=1 for read command, =0, write command), then takes control of the SDA line, and at the 9th clock cycle of SCL, sends a low-level acknowledgment signal to the host before releasing the bus. After the slave is selected, it enters different states depending on the read/write bit:

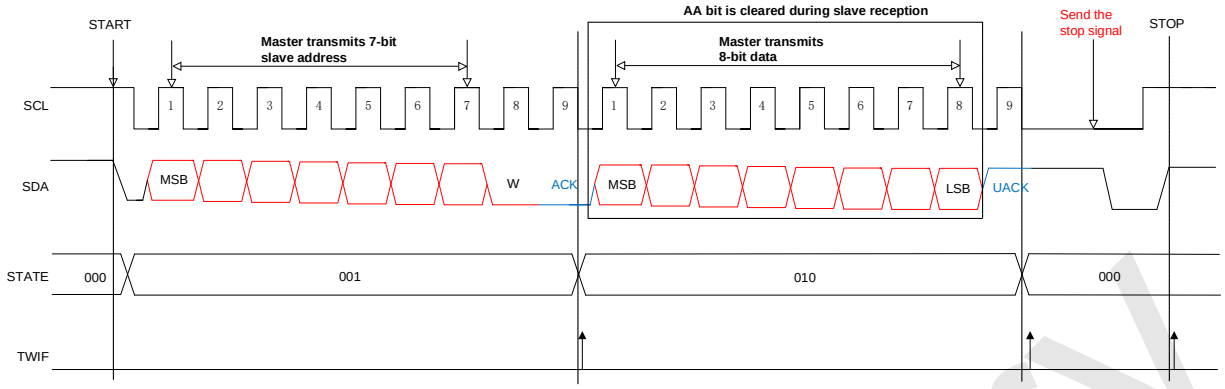
- **Non-general address response, slave receive mode**

If the read/write bit received in the first frame is write (0), the slave enters the slave receive state (STATE[2:0] = 010), waiting to receive data from the host. After the host sends 8 bits, it must release the bus and wait for the slave's acknowledgment signal during the 9th cycle.

1. If the slave's acknowledgment signal is low level, the host's communication can proceed in one of the following three ways:
   1) Continue sending data
   2) Resend the start signal. At this point, the slave re-enters the state of receiving the first frame address (STATE[2:0] = 001)
   3) Send the stop signal to indicate the end of this transmission. The slave returns to idle state, waiting for the master's next start signal.



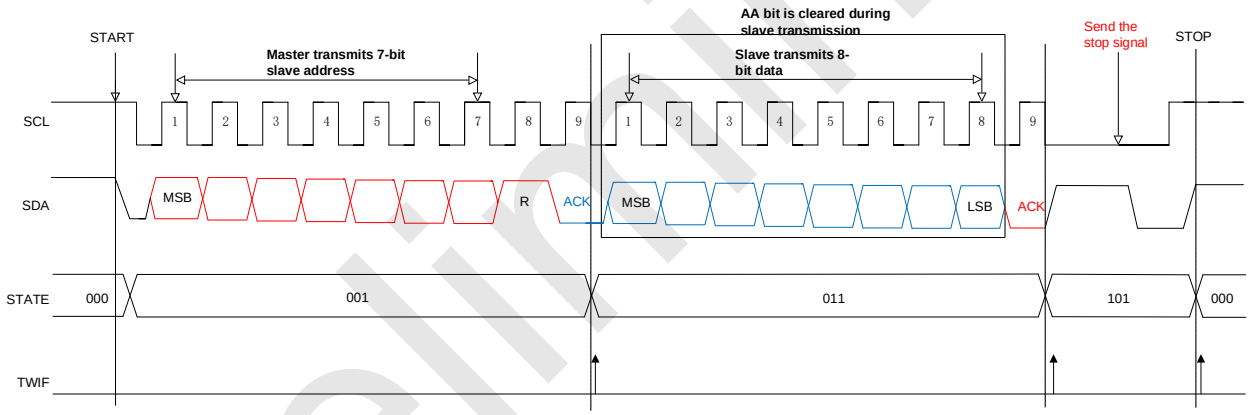
2. If the slave responds with a high logic level (during reception, the AA value in the slave register is overwritten with 0), it means that after the current byte transfer is complete, the slave will actively terminate this transmission, return to idle state (STATE[2:0] = 000), and will no longer receive data sent from the master.



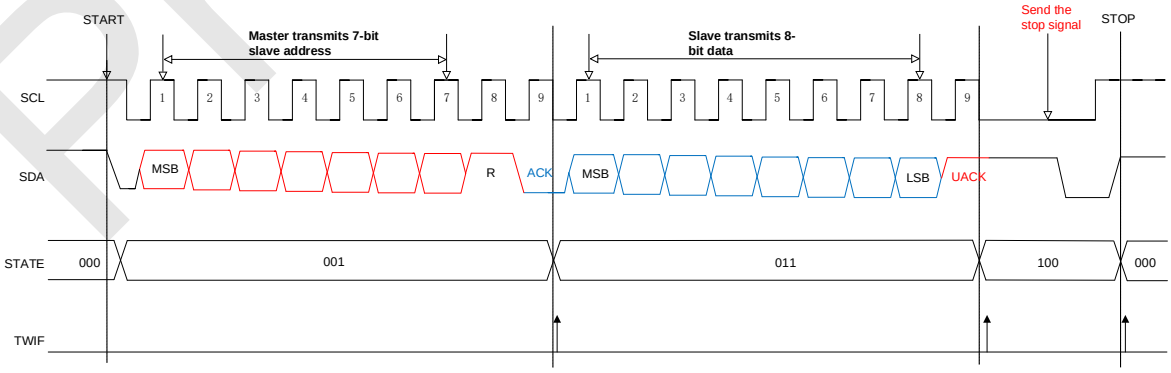
- **Non-general address response, slave transmit mode:**

If the read/write bit received in the first frame is read (1), the slave takes control of the bus and sends data to the master. After sending 8 bits of data, the slave releases the bus and waits for the master's acknowledgment:

1. If the master acknowledges with a low level, the slave continues to transmit data. During transmission, if the AA value in the slave register is overwritten to 0, the slave will actively terminate transmission after completing the current byte and release the bus, then wait for the master's stop or restart signal (STATE[2:0] = 101).



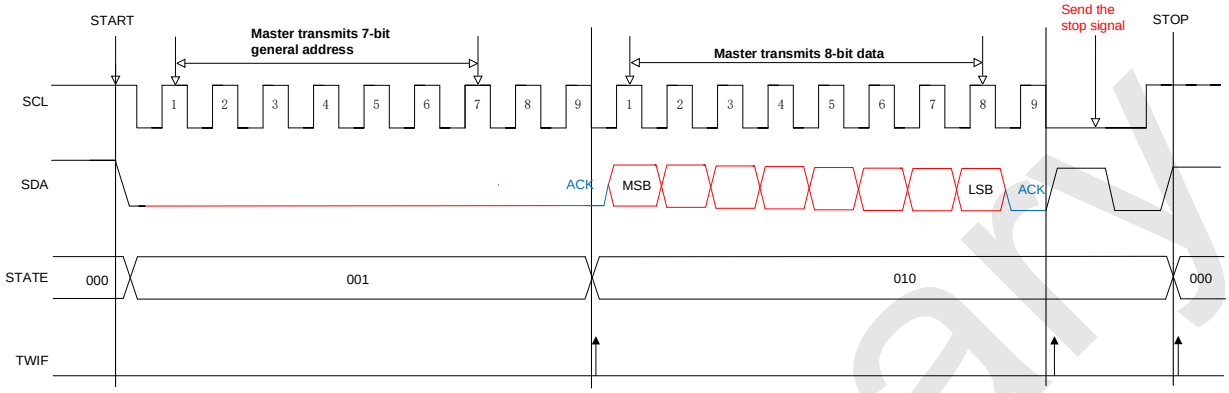
2. If the master acknowledges with a high level, the slave sets STATE[2:0] to 100 and waits for the master's stop or restart signal.



- **Response to the general address:**

When GC=1, the general address is enabled for use. The slave enters the state of receiving the first frame address (STATE[2:0] = 001). If the address bits in the first frame data are 0x00, all slaves respond to the master. The master's read/write bit must be set to write (0), causing all slaves to enter the receive data state (STATE[2:0] = 010) upon receipt. After sending every 8 bits of data, the master releases the SDA line once and reads its status:

1. If a slave acknowledges, the master's communication can proceed in one of the following three ways:
   1) Continue sending data
   2) Restart
   3) Send a stop signal to terminate the communication.



2. If no slave acknowledges, the SDA line remains idle.

Note: When using a general address in a single-master multi-slave setup, the master's read/write bit cannot be set to read (1). If set to read (1), multiple slaves would attempt to respond simultaneously, causing bus contention.

17.2.3 Procedure

The operation steps for the TWI function in the tri-mode serial port are as follows:

1. Configure SSMOD[1:0] to select TWI mode
2. Configure SSCON0 TWI control register
3. Configure SSCON1 TWI address register
4. If the slave receives data, wait for the TWIF in SSCON0 to be set. Each time the slave receives 8 bits of data, the TWIF is set and must be cleared manually
5. If the slave sends data, write the data to be sent into TWDAT, and the TWI will automatically transmit it. After sending 8 bits, the TWIF is set.

17.3 UART

SSMOD[1:0] = 11, the 3-in-1 serial interface SSI is configured as a UART interface.

SSCON0 (9DH) Serial Port 1 control register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	SM0	-	SM2	REN	TB8	RB8	TI	RI
Read/Write	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7	**SM0**	Serial communication mode control bits 0: Mode 1, 10-bit full-duplex asynchronous communication consisting of 1 start bit, 8 data bits, and 1 stop bit. variable baud rate. 1: Mode 3, 11-bit full-duplex asynchronous communication consisting of 1 start bit, 8 data bits, one programmable 9th bit, and 1 stop bit variable baud rate.

Bit Number	Bit Symbol	Description
5	**SM2**	Serial communication mode control bit 2. This bit applies only to mode 3. 0: RI is set to generate an interrupt request for each complete data frame received 1: RI is set to generate an interrupt request upon receiving a complete data frame only if RB8=1.
4	**REN**	Receive enable control bit 0: Receiving data is disabled 1: Receiving data is enabled.
3	**TB8**	Valid only in mode 3. Corresponds to the 9th bit of transmitted data
2	**RB8**	Valid only in mode 3. Corresponds to the 9th bit of received data
1	**TI**	Transmit interrupt flag. This bit is set to 1 by hardware upon transmission completion and requires software to write 1 to clear.
0	**RI**	Receive interrupt flag. This bit is set to 1 by hardware upon reception completion and requires software to write 1 to clear.
6	**-**	Reserved

SSCON1 (9EH) Serial Port 1 Baud Rate Control Register Low Byte (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BAUDL [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

SSCON2 (95H) Serial Port 1 Baud Rate Control Register High (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BAUDH [7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**BAUD [15:0]**	Serial port baud rate control $\text{BaudRate} = \frac{f_{SYS}}{\text{BAUD1H, BAUD1L}}$ **Note: [BAUD1H, BAUD1L] must be greater than 0x0010**

SSDAT (9FH) Serial Port Data Buffer Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	SBUF[7:0]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**SBUF[7:0]**	Serial port data buffer register SBUF includes two registers: a transmit shift register and a receive latch. Writing to SBUF loads data into the transmit shift register and starts the transmission process, while reading from SBUF returns the data stored in the receive latch.

18 Analog-to-Digital converter ADC

The SC92F531X integrates 22+1 channels of 12-bit high-precision successive approximation ADC. The external 22 ADC channels are multiplexed with IO port functions, and one internal channel can connect to 1/4 V_{DD}. It uses internal 1.024V, 2.4V, or 2.048V reference voltage options for measuring V_{DD}.

The SC92F531X ADC Reference Voltage offers four selectable options:

1. VDD pin (i.e., directly the internal V_{DD})
2. The internal regulator outputs a precise reference voltage of 1.024V.
3. The internal regulator outputs a precise reference voltage of 2.4V.
4. The internal regulator outputs a precise reference voltage of 2.048V.

18.1 ADC Related Registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
ADCCFG2	AAH	ADC Configuration Register 2	AINX[1:0]		-	LOWSP[2:0]			-	-	00x000xxb
ADCCFG0	ABH	ADC Configuration Register 0	EAINx[7:0]								00000000b
ADCCON	ADH	ADC Control Register	ADCEN	ADCS	ADCIF	ADCIS[4:0]					00000000b
ADCVL	AEH	ADC Result Register	ADCV[3:0]				-	-	-	-	1111xxxxb
ADCVH	AFH	ADC Result Register	ADCV[11:4]								11111111b

The following explains each register:

ADCCON (ADH) ADC Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ADCEN	ADCS	ADCIF	ADCIS[4:0]				
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	n

Bit Number	Bit Symbol	Description
7	**ADCEN**	Power supply to start the ADC 0: Turn off ADC module power 1: Turn on ADC module power
6	**ADCS**	ADC start trigger control Write "1" to this bit to start an ADC conversion. This bit acts only as the conversion trigger and only writing "1" is valid. **Note: After writing "1" to ADCS, do not perform write operations on the ADCCON register before the ADCIF flag is set**
5	**ADCIF**	ADC conversion complete flag 0: Conversion not yet complete 1: This bit is automatically set to 1 by hardware after conversion completes. Software must clear this bit
4-0	**ADCIS[4:0]**	ADC input channel selection 00000: Select AIN0 as ADC input 00001: Select AIN1 as ADC input 00010: Select AIN2 as ADC input 00011: Select AIN3 as ADC input 00100: Select AIN4 as ADC input 00101: Select AIN5 as ADC input, or OP_O as ADC input 00110: Select AIN6 as ADC input

Bit Number	Bit Symbol	Description
		00111: Select AIN7 as ADC input 01000: Select AIN8 as ADC input 01001: Select AIN9 as the ADC input 01010: Select AIN10 as the ADC input 01011: Select AIN11 as the ADC input 01100: Select AIN12 as the ADC input 01101: Select AIN13 as the ADC input 01110: Select AIN14 as the ADC input 01111: Select AIN15 as the ADC input 10000: Select AIN16 as the ADC input 10001: Select AIN17 as the ADC input 10010: Select AIN18 as the ADC input 10011: Select AIN19 as the ADC input 10100: Select AIN20 as the ADC input 10101: Select AIN21 as the ADC input 10110:-11110: Reserved 11111: ADC input is 1/4 V_{DD}, usable for measuring the power supply voltage Note: When ADCIS[4:0] = 00101, if OP is enabled and OPOSEL = 1, OP_O is selected as the ADC input otherwise, AIN5 is selected

ADCCFG2 (AAH) ADC Setting Register 2 (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AINX[1:0]		-	LOWSP[2:0]			-	-
Read/Write	R/W	R/W	-	R/W	R/W	R/W	-	-
Power-On Initial Value	0	0	x	0	0	0	x	x

Bit Number	Bit Symbol	Description
4-2	**LOWSP[2:0]**	ADC sampling time selection 100: Sampling time is 3 ADC sampling clocks, approximately 100 ns @ f_{SYS}= 32 MHz 101: Sampling time is approximately 6 ADC sampling clocks, approximately 200 ns @ f_{SYS}= 32 MHz 110: Sampling time is approximately 16 ADC sampling clocks, approximately 500 ns @ f_{SYS}= 32 MHz 111: Sampling time is approximately 32 ADC sampling clocks, approximately 1000 ns @ f_{SYS}= 32 MHz Note: 1. ADC sampling clock frequency $f_{ADC} = f_{SYS}$ 2. Total ADC time from sampling to conversion completion T_{ADC} = sampling time + conversion time, where conversion time is approximately 950 ns
7-6	**AINX[1:0]**	ADC channel pointer register For detailed description see: AINX[1:0] ADC channel pointer register:
5,1-0	**-**	Reserved

18.1.1 AINX[1:0] ADC channel pointer register

ADCCFG0 represents the addresses of four ADC channel registers ADC_CHNn (n=0-3) the currently accessed ADC channel register is determined by AINX[1:0]:

ADCCFG0 (ABH) ADC configuration register 0 (R/W)

Symbol	Address	Description	7	6	5	4	3	2	1	0
ADC_CHN	ABH	ADC channel selection register	EAINx[7:0]							

Symbol	Address @ ABH	Description	7	6	5	4	3	2	1	0
ADC_CHN2	AINX[1:0] = 10	ADC channel selection register 2	-	-	EAIN21	EAIN20	EAIN19	EAIN18	EAIN17	EAIN16
ADC_CHN1	AINX [1:0] = 01	ADC channel selection register 1	EAIN15	EAIN14	EAIN13	EAIN12	EAIN11	EAIN10	EAIN9	EAIN8
ADC_CHN0	AINX [1:0] = 00	ADC channel selection register 0	EAIN7	EAIN6	EAIN5	EAIN4	EAIN3	EAIN2	EAIN1	EAIN0

ADC_CHN0 (ABH) ADC configuration register 0 (R/W)

@ AINX [1:0] = 00

Bit Number	7	6	5	4	3	2	1	0
Symbol	EAIN7	EAIN6	EAIN5	EAIN4	EAIN3	EAIN2	EAIN1	EAIN0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

ADC_CHN1 (ABH) ADC configuration register 1 (R/W)

@ AINX [1:0] = 01

Bit Number	7	6	5	4	3	2	1	0
Symbol	EAIN15	EAIN14	EAIN13	EAIN12	EAIN11	EAIN10	EAIN9	EAIN8
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

ADC_CHN2 (ABH) ADC Setting Register 2 (R/W)

@ AINX [1:0] = 10

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	EAIN21	EAIN20	EAIN19	EAIN18	EAIN17	EAIN16
Read/Write	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**EAINx (x=0-21)**	ADC Port Setting Register 0: The AINx port cannot be used as an ADC input channel 1: The AINx port can be used as an ADC input channel. When ADCIS[4:0] selects AINx as the ADC input channel, the pull-up resistor on that port is automatically removed.

OP_CTM1 (C2H@FFH) Customer Option Register 1 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	VREFS[1:0]		-	DISJTG	-	-	-	-
Read/Write	R/W	R/W	-	R/W	-	-	-	-
Power-On Initial Value	n	n	x	n	x	x	x	x

Bit Number	Bit Symbol	Description
7-6	**VREFS[1:0]**	Reference voltage selection (initial value loaded from Code Option, user can modify settings) 00: Set ADC vref to V_{DD} 01: Set ADC vref to internal accurate 1.024 V 10: Set ADC vref to internal accurate 2.4 V 11: Sets the ADC's vref to accurate internal 2.048 V

ADCVL (AEH) ADC Conversion Value Register (Low Byte) (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ADCV[3:0]				-	-	-	-
Read/Write	R/W	R/W	R/W	R/W	-	-	-	-
Power-On Initial Value	1	1	1	1	x	x	x	x

ADCVH (AFH) ADC Conversion Value Register (High Byte) (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ADCV[11:4]							
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	1	1	1	1	1	1	1	1

Bit Number	Bit Symbol	Description
11-4	**ADCV[11:4]**	High 8 bits of the ADC conversion value
3-0	**ADCV[3:0]**	Lower 4 bits of the ADC conversion value

IE (A8H) Interrupt Enable Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	EA	EADC	ET2	EUART	ET1	EINT1	ET0	EINT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
6	**EADC**	ADC conversion complete Interrupt enable control 0: Interrupt generation disabled 1: Interrupt generation enabled

IP (B8H) Interrupt Priority Control Register (R/W)

Bit Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	-	IPADC	IPT2	IPUART0	IPT1	IPINT1	IPT0	IPINT0
Read/Write	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
6	**IPADC**	ADC interrupt priority selection 0: Set ADC interrupt priority to "Low" 1: Set ADC interrupt priority to "High"

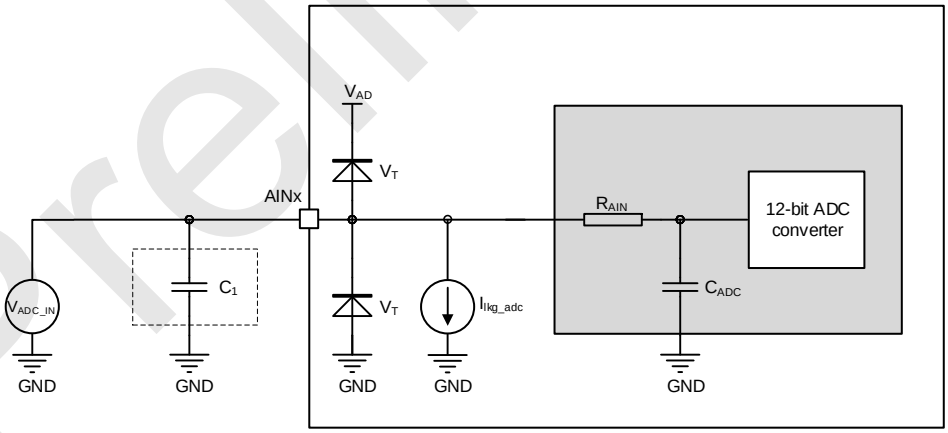
18.2 ADC conversion steps

The following steps are required for the user to perform ADC conversion:

1. Set the ADC input pin: Select AINx as the ADC input using the ADC channel pointer register AINX[1:0], combined with the ADCCFG0 register (the ADC pin is usually preset)
2. Set the ADC reference voltage (Vref)
3. Configure sampling time: Set the ADC sampling time through LOWSP[2:0]
4. Enable the ADC module power supply. Select the ADC input channel: set the ADCIS bit to choose the ADC input channel
5. Start the conversion: set the ADCS bit to begin conversion
6. Wait for the conversion to complete: wait until the ADCIF flag is set. If ADC interrupt is enabled (EADC=1), the ADC interrupt will be triggered
7. Read the conversion result: read the 12-bit conversion result from the ADCVH and ADCVL registers (high byte first, then low byte), completing the conversion
8. Proceed to the next conversion: if the input channel is not changed, repeat steps 6 through 8.

Note: Before enabling the interrupt by setting IE[6] (EADC), it is recommended to clear the ADCIF flag by software first. After the ADC interrupt service routine completes, clear the ADCIF flag to avoid frequent interrupts.

18.3 ADC connection circuit diagram



Note:

1. C1 is an external 0.01μF capacitor. Users should add this capacitor to improve ADC performance
2. For ADC-related electrical parameters, see ADC electrical characteristics.

19 OP/CMP Two-in-one analog operational amplifier module

The SC92F531X integrates an OP/CMP two-in-one analog operational amplifier module, allowing users to select either analog comparator or operational amplifier mode. The specific configuration method is as follows:

ZOCINX (B4H) ZOC index register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	ZOCMOD[1:0]		-	-	-	-	-	-
Read/Write	R/W	R/W	-	-	-	-	-	-
Power-On Initial Value	0	0	x	x	x	x	x	x

Bit Number	Bit Symbol	Description
7-6	**ZOCMOD[1:0]**	**ZOC dual-select mode control bit** 00: ZOC off 01: Reserved 10: ZOC set to CMP mode 11: ZOC set to OP mode
5-0	**-**	Reserved

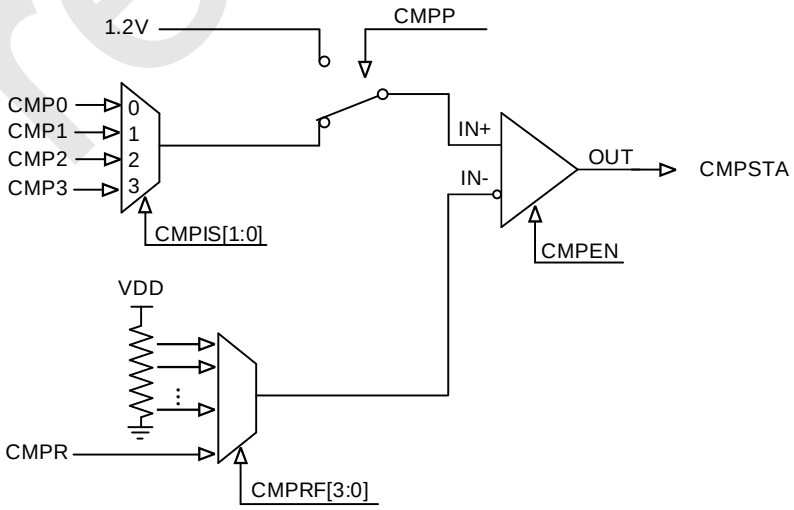
19.1 Analog comparator (CMP)

When ZOCMOD[1:0]=10, the dual-function module operates as an analog comparator, and the CMP interrupt can wake the device from STOP mode.

This comparator has five analog signal positive input terminals: four external (CMP0 to CMP3) and one internal (1.2V reference voltage), selectable via CMPP and CMPIS[1:0]. The negative input voltage can be switched via CMPRF[3:0] to either the external voltage on the CMPR pin or one of fifteen levels of internal comparison voltage.

The comparator interrupt mode can be conveniently set with CMPIM[1:0]. When the interrupt condition set by CMPIM[1:0] occurs, the comparator interrupt flag CMPIF is set and must be cleared by software.

19.1.1 Analog comparator block diagram



Analog comparator block diagram

19.1.2 Analog comparator related registers

ZOCCON (B7H) Analog comparator control register (R/W) (ZOCMOD = 10)

Bit Number	7	6	5	4	3	2	1	0
Symbol	CMPEN	CMPIF	CMPSTA	-	CMPRF[3:0]			
Read/Write	R/W	R/W	R/W	-	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	x	0	0	0	0

Bit Number	Bit Symbol	Description
7	**CMPEN**	Analog comparator enable control bit 0: Disable the analog comparator 1: Enable the analog comparator
6	**CMPIF**	Analog comparator interrupt flag bit 0: Comparator interrupt not triggered 1: This bit is set to 1 automatically by hardware when the comparator meets the interrupt trigger condition. If IE1[5] (ECMP) is also set to 1, the comparator interrupt will be generated. After the comparator interrupt occurs, this bit is not automatically cleared by hardware and must be cleared by software.
5	**CMPSTA**	Analog comparator output status 0: Comparator non-inverting input voltage is less than inverting input voltage 1: Comparator non-inverting input voltage is greater than inverting input voltage
3-0	**CMPRF[1:0]**	Analog comparator inverting input reference voltage selection: 0000: Select CMPR as the comparator reference voltage for the analog comparator 0001: Select 1/16V_{DD} as the comparator reference voltage for the analog comparator 0010: Select 2/16V_{DD} as the comparator reference voltage for the analog comparator 0011: Select 3/16V_{DD} as the comparator reference voltage for the analog comparator 0100: Select 4/16V_{DD} as the comparator reference voltage for the analog comparator 0101: Select 5/16V_{DD} as the comparison voltage for the analog comparator. 0110: Select 6/16V_{DD} as the comparison voltage for the analog comparator. 0111: Select 7/16V_{DD} as the comparison voltage for the analog comparator. 1000: Select 8/16V_{DD} as the comparison voltage for the analog comparator. 1001: Select 9/16V_{DD} as the comparison voltage for the analog comparator. 1010: Select 10/16V_{DD} as the comparison voltage for the analog comparator. 1011: Select 11/16V_{DD} as the comparison voltage for the analog

Bit Number	Bit Symbol	Description
		comparator. 1100: Select 12/16V_{DD} as the comparison voltage for the analog comparator. 1101: Select 13/16V_{DD} as the comparison voltage for the analog comparator 1110: Select 14/16V_{DD} as the comparison voltage for the analog comparator 1111: Select 15/16V_{DD} as the comparison voltage for the analog comparator
4	-	Reserved

ZOCCFG (B6H) Analog comparator configuration register (R/W) (ZOCMOD = 10)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	CMPP	CMPIM[1:0]		CMPIS[1:0]	
Read/Write	-	-	-	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	x	0	0	0	0	0

Bit Number	Bit Symbol	Description
4	**CMPP**	Analog comparator positive input selection 0: The analog comparator positive input is one of CMP0-3, as set by CMPIS[1:0] 1: The analog comparator positive input is the internal 1.2V reference voltage
3-2	**CMPIM[1:0]**	Analog comparator interrupt mode selection 00: No interrupt 01: Rising edge interrupt: An interrupt occurs when IN+ changes from less than IN- to greater than IN-. 10: Falling edge interrupt: An interrupt occurs when IN+ changes from greater than IN- to less than IN-. 11: Dual-edge interrupt: An interrupt occurs when IN+ changes from less than IN- to greater than IN-, or from greater than IN- to less than IN-.
1-0	**CMPIS[1:0]**	Analog comparator positive input channel selection. This bit is invalid when CMPP = 1 00: Select CMP0 as the analog comparator positive input. 01: Select CMP1 as the analog comparator positive input. 10: Select CMP2 as the analog comparator positive input. 11: Select CMP3 as the analog comparator positive input.
5	-	Reserved

19.2 Operational amplifier (OP)

When ZOCMOD[1:0] = 11, the two-in-one module operates as an operational amplifier.

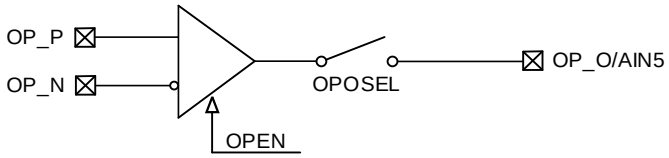
OP_O is multiplexed with ADC channel AIN5. Users can configure the following to sample the OP_O output via ADC:

1. 1. Set OPOSEL = 1 to enable the path from OP_O to the multiplexed pin.

2. 2. Set ADCIS[4:0] = 00101 (select AIN5) to have the ADC sample the signal from the multiplexed pin.

After completing these configurations, the ADC will directly sample the output of OP_O.

19.2.1 Operational Amplifier Block Diagram



Note: When using the SC92F531X operational amplifier, users must connect external feedback resistors as required.

19.2.2 Operational Amplifier Related Registers

ZOCCON (B7H) OP Setting Register (R/W) (ZOCMOD = 11)

Bit Number	7	6	5	4	3	2	1	0
Symbol	OPEN		-	-	-	-	-	OPOSEL
Read/Write	R/W	-	-	-	-	-	-	R/W
Power-On Initial Value	0	x	x	x	x	x	x	0

Bit Number	Bit Symbol	Description
7	**OPEN**	Operational amplifier enable control bit 0: Disable the operational amplifier 1: Enable the operational amplifier
0	**OPOSEL**	OP output connection selection bit 0: Disconnected from OP_O 1: OP output connected to OP_O
6-1	**-**	Reserved

20 Checksum module

The SC92F531X includes a built-in checksum module that can generate a 16-bit checksum value of the program code in real time. Users can compare this checksum with the theoretical value to verify whether the contents of the program area are correct.

Note: The checksum value is the cumulative sum of all data within the entire program area, specifically from address 0000H to 1FFDH. If residual data from previous user operations remain in any address unit, the checksum will differ from theoretical value. Therefore, it is recommended that users erase the entire code area or write zeros to it before programming the code to ensure the checksum matches the theoretical value.

20.1 Checksum verification-related registers

CHKSUML (FCH) Checksum Result Register Low Byte (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	CHKSUML[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**CHKSUML [7:0]**	Checksum Result Register Low Byte

CHKSUMH (FDH) Checksum Result Register High Byte (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	CHKSUMH[7:0]							
Read/Write	R	R	R	R	R	R	R	R
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**CHKSUMH [7:0]**	Checksum Result Register High Byte

OPERCON (EFH) Operation Control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	OPERS	MD	-	-	-	-	-	CHKSUMS
Read/Write	R/W	R/W	-	-	-	-	-	R/W
Power-On Initial Value	0	0	x	x	x	x	x	0

Bit Number	Bit Symbol	Description
0	**CHKSUMS**	Checksum start trigger control Write “1” to this bit to start one Checksum calculation. Only writing 1 is valid

21 LED drive

21.1 Features

- A total of 8 LED driver ports: LED0 to LED7
- All LED ports support 16-level source drive control
- LED0 to LED7 driver pins can supply 130mA @ 0.8V high current drive
- IC system clock (f_{SYS}) as LED clock source
- After completing one LED frame scan, the corresponding LED driver flag AUIF is set
- During automatic scanning, the output period width of SEG is equal to that of COM
- LED dead time is configurable
- Characteristics of the LED bidirectional drive mode are as follows:
  - LED0 to LED7 support bidirectional drive mode, capable of jointly driving up to 7x8 pixels
  - Scan modes selectable in eight options ranging from 7x8 to 1x2 and 1x1
  - The COM function on any LEDn port can be disabled, rendering its COM functionality inactive during scanning without affecting its role as a SEG port. This approach can increase the brightness of the LED array
  - Common COM ports LED0/LED1/LED6/LED7 support four selectable scanning intervals: 0.5T, 1T, 1.5T, and 2T

21.2 LED-related pins

P2.7	LED0
P2.6	LED1
P2.5	LED2
P2.4	LED3
P2.3	LED4
P2.2	LED5
P2.1	LED6
P2.0	LED7

21.3 LED display driver related registers

Symbol	Address	Description	7	6	5	4	3	2	1	0	Power-On Initial Value
LEDVO0	9CH	LED Display Driver Output Register	LED7VO	LED6VO	LED5VO	LED4VO	LED3VO	LED2VO	LED1VO	LED0VO	00000000b
COMCON	A4H	COM Port Control Register	COMFB7	COMFB6	COMFB5	COMFB4	COMFB3	COMFB2	COMFB1	COMFB0	00000000b
DDRCON2	A6H	Display Driver Control Register 2	-	-	-	-	DRIV[3:0]				xxxx1111b
DDRCON0	96H	Display Driver Control Register	DDRON	-	-	-	-	-	-	-	0xxxxxxxb
SCANCON	97H	Display Driver Scan Configuration Register	AUIF	CMEN	LEDXT[1:0]		LTSEL[1:0]		DISPCK [1:0]		00010000b

The following explains each register:

21.3.1 DDRCON0(96H) Display driver control register 0 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	DDRON	-	-	-	-	-	-	-
Read/Write	R/W	-	-	-	-	-	-	-
Power-On Initial Value	0	x	x	x	x	x	x	x

Bit Number	Bit Symbol	Description
7	**DDRON**	LED display driver enable control 0: Display driver scanning off 1: Display driver scanning on, constant current source enabled synchronously

21.3.2 LEDVO0 (9CH) LED display drive output Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	LED7VO	LED6VO	LED5VO	LED4VO	LED3VO	LED2VO	LED1VO	LED0VO
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**LEDnVO** **n=0-7**	Enable LEDn port display drive output 0: Disable the display drive output function of the LEDn port 1: Enable the display drive output function of the LEDn port **Note: In bidirectional drive mode, the scan count depends on the number of LEDn functions selected.** ● For example: ■ Bidirectional drive mode: User enables 5 LED drive ports, actual scan duty is 1/5 ■ In normal mode: User enables 3 COMs, actual scan duty is 1/3

21.3.3 COMCON (A4H) COM control Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	COMFB7	COMFB6	COMFB5	COMFB4	COMFB3	COMFB2	COMFB1	COMFB0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	0	0	0	0	0

Bit Number	Bit Symbol	Description
7-0	**COMFBn** **n=0-7**	COM disable bit In bidirectional drive mode, mask LEDn ports as COM to prevent them from acting as COM and allow them only as SEG ports 0: LEDn port can serve as a COM port 1: LEDn port cannot serve as a COM port, only as a SEG port

21.3.4 DDRCON2 (A6H) Display drive control Register 2 (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	DRIV[3:0]			
Read/Write	-	-	-	-	R/W	R/W	R/W	R/W
Power-On Initial Value	x	x	x	x	1	1	1	1

Bit Number	Bit Symbol	Description
3-0	**DRIV[3:0]**	Constant current source output current selection bit Higher the DRIV[3:0] values increase current. Lower values decrease current. Power-On Initial Value is 1111: 20mA Constant current source setting applies to all enabled LED ports

Serial Number	DRIV[3:0]	Parameter
0	0000	Brightness Level 1
1	0001	Brightness Level 2
2	0010	Brightness Level 3
3	0011	Brightness Level 4
4	0100	Brightness Level 5
5	0101	Brightness Level 6
6	0110	Brightness Level 7
7	0111	Brightness Level 8
8	1000	Brightness Level 9
9	1001	Brightness Level 10
10	1010	Brightness Level 11
11	1011	Brightness Level 12
12	1100	Brightness Level 13
13	1101	Brightness Level 14
14	1110	Brightness Level 15
15	1111	Brightness Level 16

21.3.5 SCANCON (97H) Display Driver Scan Configuration Register (R/W)

Bit Number	7	6	5	4	3	2	1	0
Symbol	AUIF	CMEN	LEDXT[1:0]		LTSEL[1:0]		DISPCK[1:0]	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-On Initial Value	0	0	0	1	0	0	0	0

Bit Number	Bit Symbol	Description
7	**AUIF**	One frame scan completion flag 0: Scan not completed 1: One frame scan completed. This bit is set by hardware and cleared to 0 by software writing 1
6	**CMEN**	IO port constant current output mode enable bit 0: IO constant current output mode not enabled 1: IO constant current output mode enabled
5-4	**LEDXT[1:0]**	LED-specific scan port scan time setting bits 00: 0.5T

<table>
<tr><th>Bit Number</th><th>Bit Symbol</th><th>Description</th></tr>
<tr><td></td><td></td><td>01: 1T — Power-On Initial Value
10:1.5T
11:2T

Note:
1. LED specific scanning port is set by LTSEL[1:0]
2. When bidirectional drive mode is selected, the display mode defaults to 7-segment x 8-digit, and the scan time defaults to "1T"
3. The scan time setting only applies to the specific scanning port selected by LTSEL[1:0], while the scan time for other LEDn ports is fixed at "1T"

“1T” is approximately equal to the duration of one LED clock cycle (as set by DISPCK[1:0]).</td></tr>
<tr><td>3-2</td><td>LTSEL[1:0]</td><td>LED specific scanning port selection bits:
00:LED0
01:LED1
10:LED6
11:LED7
The scan time of the selected LEDn (n=0, 1, 6, 7) changes according to the LEDXT[1:0] setting</td></tr>
<tr><td>1-0</td><td>DISPCK[1:0]</td><td>LED module clock division:
The clock source is the system clock f_{SYS}, with the following division levels:
00:f_{SYS} / 4096
01:f_{SYS} / 8192
10:f_{SYS} / 16384
11:f_{SYS} / 32768

Note: The LED dead time depends on DISPCK[1:0]. The dead time reference is as follows: (To ensure better display quality, LED dead time can be set between 11μs and 3μs)
<table>
<tr><th>DISPCK[1:0]</th><th>f_{SYS}=8 MHz</th><th>f_{SYS}=16 MHz</th><th>f_{SYS}=32 MHz</th><th>Unit</th></tr>
<tr><td>= 00</td><td>4</td><td>2</td><td>1</td><td rowspan="4">μs</td></tr>
<tr><td>= 01</td><td>8</td><td>4</td><td>2</td></tr>
<tr><td>= 10</td><td>16</td><td>8</td><td>4</td></tr>
<tr><td>= 11</td><td>32</td><td>16</td><td>8</td></tr>
</table>
</td></tr>
</table>

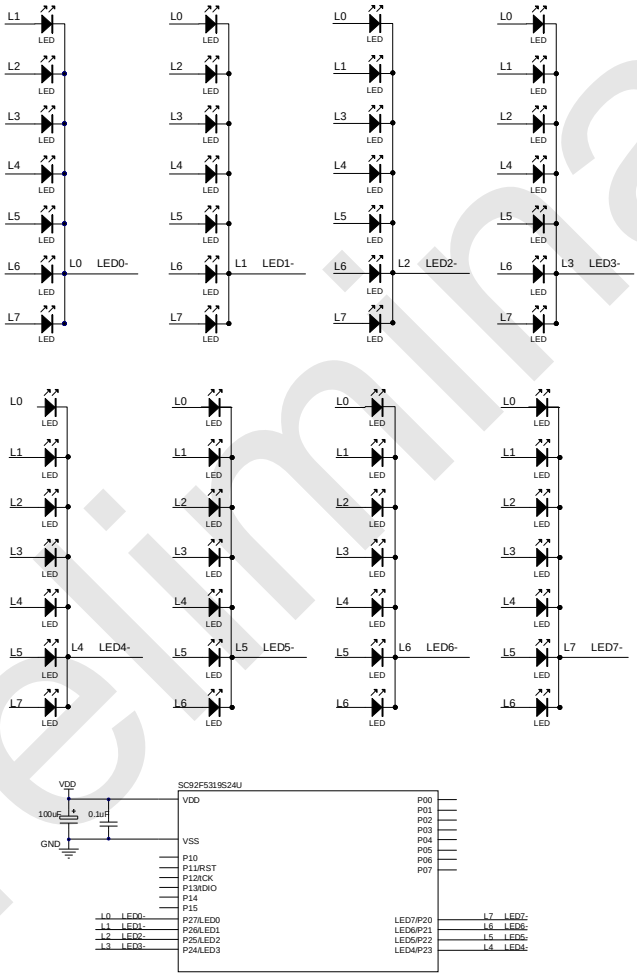
21.4 Bidirectional drive LED display RAM

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
100H	LED0-	7	6	5	4	3	2	1	-
101H	LED1-	15	14	13	12	11	10	-	0
102H	LED2-	23	22	21	20	19	-	9	8
103H	LED3-	31	30	29	28	-	18	17	16

Address	Register Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
104H	LED4-	39	38	37	-	27	26	25	24
105H	LED5-	47	46	-	36	35	34	33	32
106H	LED6-	55	-	45	44	43	42	41	40
107H	LED7-	-	54	53	52	51	50	49	48

21.4.1 Hardware connection example for bidirectional drive mode LED

In the illustration below, Ln represents the segment output of LEDn, with a constant current effective output LEDn- corresponds to the bit scan of LEDn, with an active low level.



Hardware connection example for bidirectional drive mode LED

During the active scanning period of LEDn-, the LEDn driver outputs a low-level signal (n=0, 1, 2…7), while signals from other LED drivers are determined by the display data:

- When the display data is “1”, the corresponding LED driver outputs a high-level signal
- When the displayed data is “0”, the corresponding LED driver enters a high impedance (floating) state
- When scanning LEDn-, the corresponding LEDn- outputs a low level

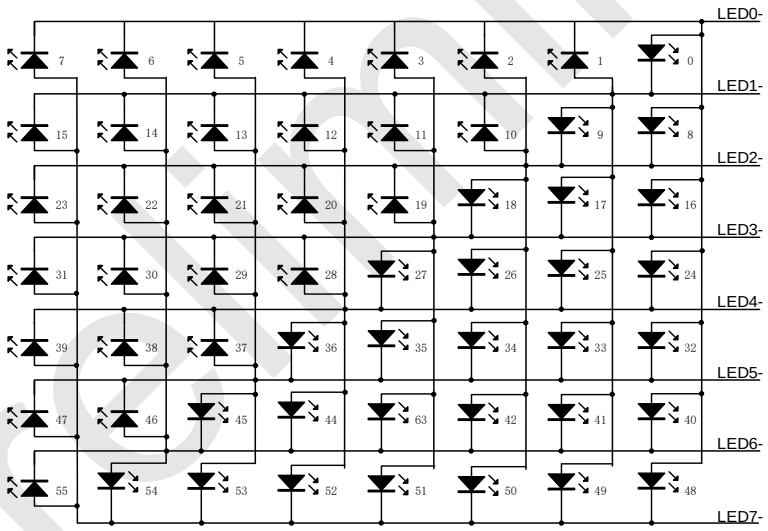
To prevent LED flicker caused by switching the LEDn- scanning interval, the LED driver includes a fixed dead time. During the dead time, the LED driver briefly outputs an inactive signal.

The correspondence between display data, address, and chip pins (LEDn) is shown in the table below (Ln is the segment output corresponding to LEDn, with constant current as the effective output. LEDn- is the bit scan corresponding to LEDn, with the effective level being low):

bit	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	LEDn Port Scanning
Address	L7	L6	L5	L4	L3	L2	L1	L0	
100H	7	6	5	4	3	2	1	-	LED0-
101H	15	14	13	12	11	10	-	0	LED1-
102H	23	22	21	20	19	-	9	8	LED2-
103H	31	30	29	28	-	18	17	16	LED3-
104H	39	38	37	-	27	26	25	24	LED4-
105H	47	46	-	36	35	34	33	32	LED5-
106H	55	-	45	44	43	42	41	40	LED6-
107H	-	54	53	52	51	50	49	48	LED7-

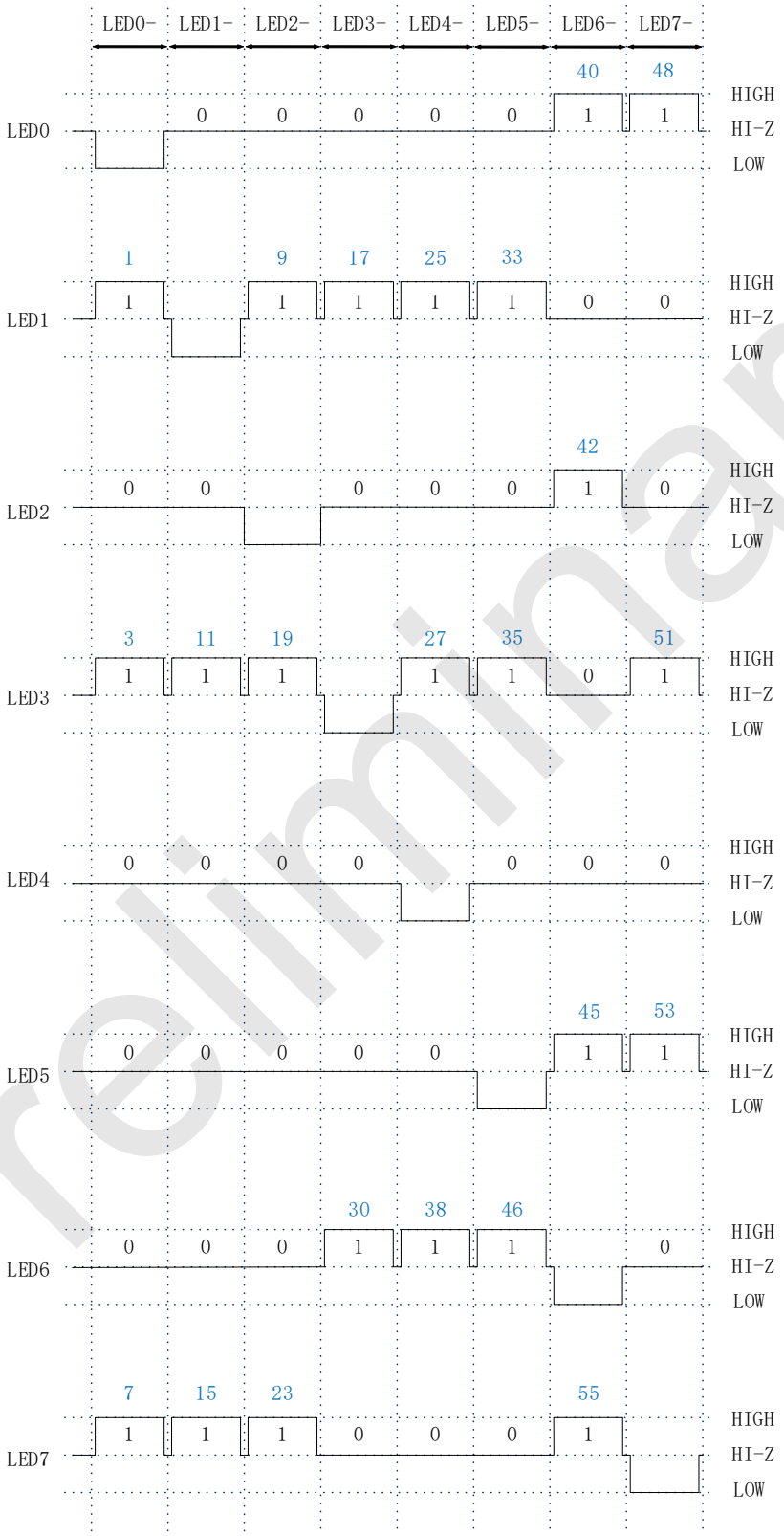
In the table above, the numbers in the white cells correspond one-to-one to the LED numbers shown in the figure below:

21.4.2 Forward and reverse scanning timing



21.4.3 Example of scanning timing

The blue numbers in the figure below correspond to the LED numbers in the forward and reverse scanning timing diagram. The LEDs lit during scanning from LED0 to LED7 are as follows:



The forward and reverse scanning timing diagram

22 Electrical characteristics

22.1 Absolute maximum ratings

Symbol	Parameter	Minimum Value	Maximum Value	Unit
V_{DD}	DC Supply Voltage	-0.3	6	V
V_{PIN}	Input/Output Voltage for Any Pin	-0.3	V_{DD}+0.3	V
T_A	Operating Ambient Temperature	-40	105	℃
T_{STG}	Storage Temperature	-55	125	℃
I_{VDD}	Current Through VDD	-	200	mA
I_{VSS}	Current Through VSS	-	200	mA

22.2 Recommended operating conditions

Symbol	Parameter	Minimum Value	Maximum Value	Unit
V_{DD}	Operating Voltage	2.4	5.5	V
T_A	Operating Ambient Temperature	-40	105	℃

22.3 Flash rom parameters

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{Write}	Write Voltage	4.5	5	5.5	V	
N_{END}	Erase/Write Cycles	1000	-	-	Cycles	V_{DD} = 5.0 V T_A = +25 ℃
T_{DR}	Data Retention Time	10	-	-	Years	T_A = +25 ℃

22.4 EEPROM parameters

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{Read}	Read Voltage	2.4		5.5	V	
V_{Write}	Write Voltage	2.5		5.5	V	
N_{END}	Erase/Write Cycles	10,000	-	-	Cycles	
T_{DR}	Data Retention Time	10	-	-	Years	V_{DD} = 5.0V T_A = +125℃
T_{Write}	Single Byte Write Time	-	4	-	ms	V_{DD} = 5.0V T_A = +25℃ PAYTIMES[1:0] = 00

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
		-	2	-	ms	V_{DD} = 5.0V T_A = +25℃ PAYTIMES[1:0] = 01
		-	1	-	ms	V_{DD} = 5.0V T_A = +25℃ PAYTIMES[1:0] = 10

22.5 DC electrical characteristics

(V_{DD} = 5V, T_A = +25℃, unless otherwise specified)						
Symbol	**Parameter**	**Minimum Value**	**Typical Value**	**Maximum Value**	**Unit**	**Condition**
I_{op}	Operating Current in Operation Mode	-	3.8	-	mA	f_{SYS} =32 MHz
		-	2.9	-	mA	f_{SYS} =16 MHz
		-	2.4	-	mA	f_{SYS} =8 MHz
		-	2.1	-	mA	f_{SYS} =2.66 MHz
I_{IDL}	Operating Current in IDLE Mode	-	2.1	-	mA	f_{SYS} =32 MHz
		-	1.4	-	mA	f_{SYS} =2.66 MHz
I_{pd}	Operating Current in STOP mode	-	2	-	μA	
I_{BTM}	Operating Current in Base Timer Mode	-	0.9	2	μA	BTMFS[3:0]=1000 An Interrupt is generated every 4.0 s
I_{WDT}	WDT Current	-	0.9	2	μA	WDTCKS[2:0]=000 WDT overflow time 500 ms

(V_{DD} = 3.3V, T_A = +25℃, unless otherwise specified)						
Symbol	**Parameter**	**Minimum Value**	**Typical Value**	**Maximum Value**	**Unit**	**Condition**
I_{op}	Operating Current in Operation Mode	-	3.3	-	mA	f_{SYS} =32 MHz
		-	2.6	-	mA	f_{SYS} =16 MHz
		-	2.2	-	mA	f_{SYS} =8 MHz
		-	2	-	mA	f_{SYS} =2.66 MHz
I_{IDL}	Operating Current in IDLE Mode	-	2.1	-	mA	f_{SYS} =32 MHz
		-	1.3	-	mA	f_{SYS} =2.66 MHz
I_{pd}	Operating Current in STOP mode	-	1.8	-	μA	
I_{BTM}	Operating Current in Base Timer Mode	-	0.8	2	μA	BTMFS[3:0]=1000 An Interrupt is generated every 4.0 s
I_{WDT}	WDT Current	-	0.8	2	μA	WDTCKS[2:0]=000 WDT overflow time 500 ms

22.6 IO port electrical characteristics

IO port characteristics (VDD = 5V, TA = +25℃, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{IH1}	Input high Voltage	$0.7V_{DD}$	-	V_{DD}+0.3	V	
V_{IL1}	Input low Voltage	-0.3	-	$0.3V_{DD}$	V	
V_{IH2}	Input high Voltage Note 1	$0.8V_{DD}$	-	V_{DD}	V	
V_{IL2}	Input low Voltage Note 1	-0.2	-	$0.2V_{DD}$	V	
I_{OL1}	Output low current P0 and P1 ports	-	43	-	mA	V_{Pin} =0.4 V
		-	82	-	mA	V_{Pin} =0.8 V
I_{OL2}	Output low current P2 port (LED multiplexed port), DRV_EH = 0	-	43	-	mA	DRV_EH = 0 V_{Pin} =0.4 V
		-	82	-	mA	DRV_EH = 0 V_{Pin} =0.8 V
I_{OL3}	Output low current P2 port (LED multiplexed port), DRV_EH = 1	-	68	-	mA	DRV_EH = 1 V_{Pin} =0.4 V
		-	126	-	mA	DRV_EH = 1 V_{Pin} =0.8 V
I_{LED_OL}	LED pin sourcing current (per pin)	-	68	-	mA	V_{LED} = 0.4 V
		-	126	-	mA	V_{LED} = 0.8 V
I_{OH1}	Output high current	-	22	-	mA	V_{Pin}=4.3 V
I_{OH2}	Output high current	-	9	-	mA	V_{Pin}=4.7 V
I_{lkg}	Input leakage current	-1	-	1	μA	IO in high-impedance input mode V_{IN}= V_{DD} or V_{SS}
R_{PH}	Pull-up resistor	16.5	33	49.5	kΩ	V_{IN} = V_{SS}

Note 1: Schmitt trigger input ports include NRST T_CLK / T_DIO UART RXD SPI / TWI input signals INT0 through INT15 PWM fault detection port FLT Timer clock input Tn and Timer capture input TnEX.

IO Port Characteristics (VDD = 3.3V, TA = +25℃, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{IH1}	Input high Voltage	$0.7V_{DD}$	-	V_{DD}+0.3	V	
V_{IL1}	Input low Voltage	-0.3	-	$0.3V_{DD}$	V	
V_{IH2}	Input high Voltage Note 1	$0.8V_{DD}$	-	V_{DD}	V	
V_{IL2}	Input low Voltage Note 1	-0.2	-	$0.2V_{DD}$	V	
I_{OL1}	Output low current P0 and P1 ports	-	33	-	mA	V_{Pin} =0.4 V
		-	58	-	mA	V_{Pin}=0.8 V
I_{OL2}	Output low current P2 port (LED multiplexed port), DRV_EH = 0	-	33	-	mA	DRV_EH = 0 V_{Pin} =0.4 V
		-	58	-	mA	DRV_EH = 0 V_{Pin} =0.8 V

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
I_{OL3}	Output low current P2 port (LED multiplexed port), DRV_EH = 1	-	52	-	mA	DRV_EH = 1 V_{Pin} =0.4 V
		-	91	-	mA	DRV_EH = 1 V_{Pin} =0.8 V
I_{LED_OL}	LED pin sourcing current (per pin)	-	52	-	mA	V_{LED}=0.4 V
		-	91	-	mA	V_{LED}=0.8 V
I_{OH3}	Output high current	-	6.5	-	mA	V_{Pin}=3.0 V
I_{lkg}	Input leakage current	-1	-	1	μA	IO in high-impedance input mode V_{IN}= V_{DD} or V_{SS}
R_{PH}	Pull-up resistor	28	56	84	kΩ	V_{IN} = V_{SS}

Note 1: Schmitt trigger input ports include NRST T_CLK / T_DIO UART RXD SPI / TWI input signals INT0 through INT15 PWM fault detection port FLT Timer clock input Tn and Timer capture input TnEX.

22.7 LED electrical characteristics

(VDD = 5V, TA = +25℃, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
D_{LED_OUT}	Output Current Deviation	-	-	±5%	mA	V_{LED} = 2 V
ΔI1	Line Regulation	-	-	±3	%/V	
ΔI2	Load Regulation	-	-	±3	%/V	
ΔT	Temperature Drift	-	-	±3	%/V	

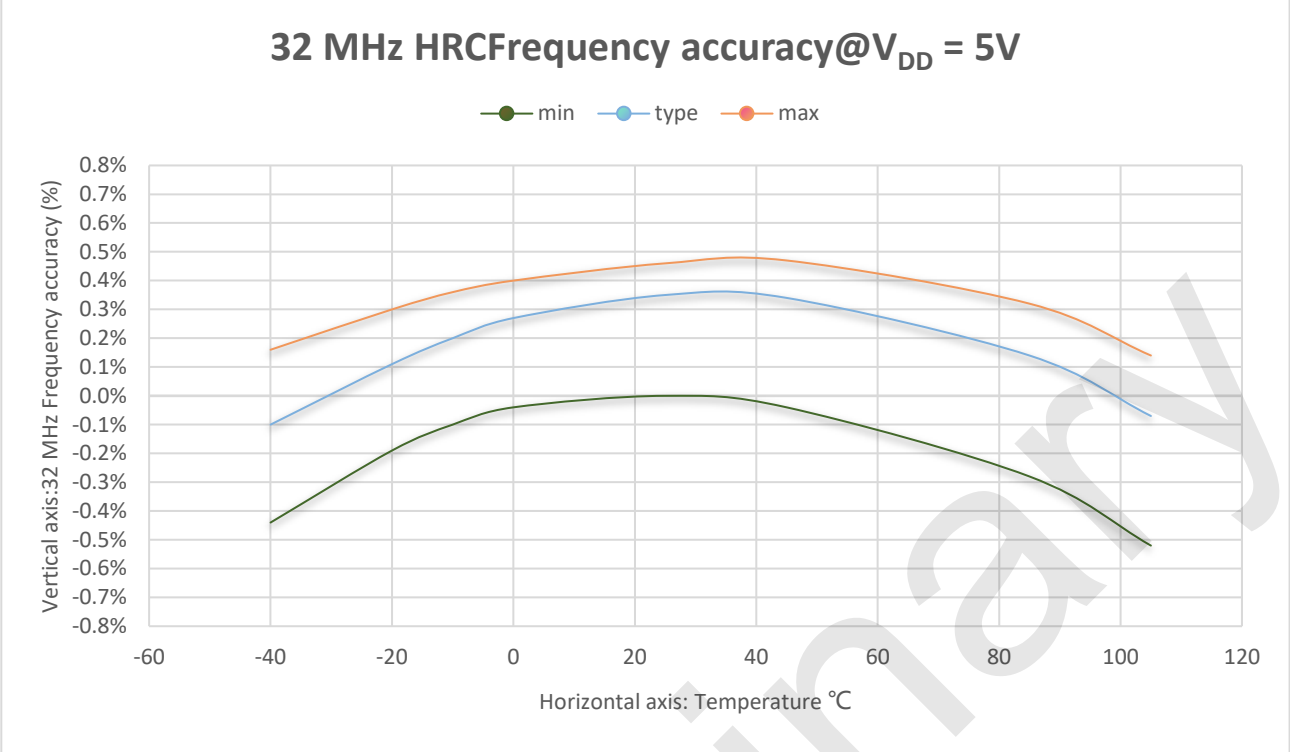
Symbol	Serial Number	DRIV[3:0]	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
I_{LED_OH}	0	0000	Brightness Level 1	-	1.25	-	mA	V_{LED} = 2 V
	1	0001	Brightness Level 2	-	2.50	-	mA	
	2	0010	Brightness Level 3	-	3.75	-	mA	
	3	0011	Brightness Level 4	-	5.00	-	mA	
	4	0100	Brightness Level 5	-	6.25	-	mA	
	5	0101	Brightness Level 6	-	7.50	-	mA	
	6	0110	Brightness Level 7	-	8.75	-	mA	
	7	0111	Brightness Level 8	-	10.00	-	mA	
	8	1000	Brightness Level 9	-	11.25	-	mA	
	9	1001	Brightness Level 10	-	12.50	-	mA	

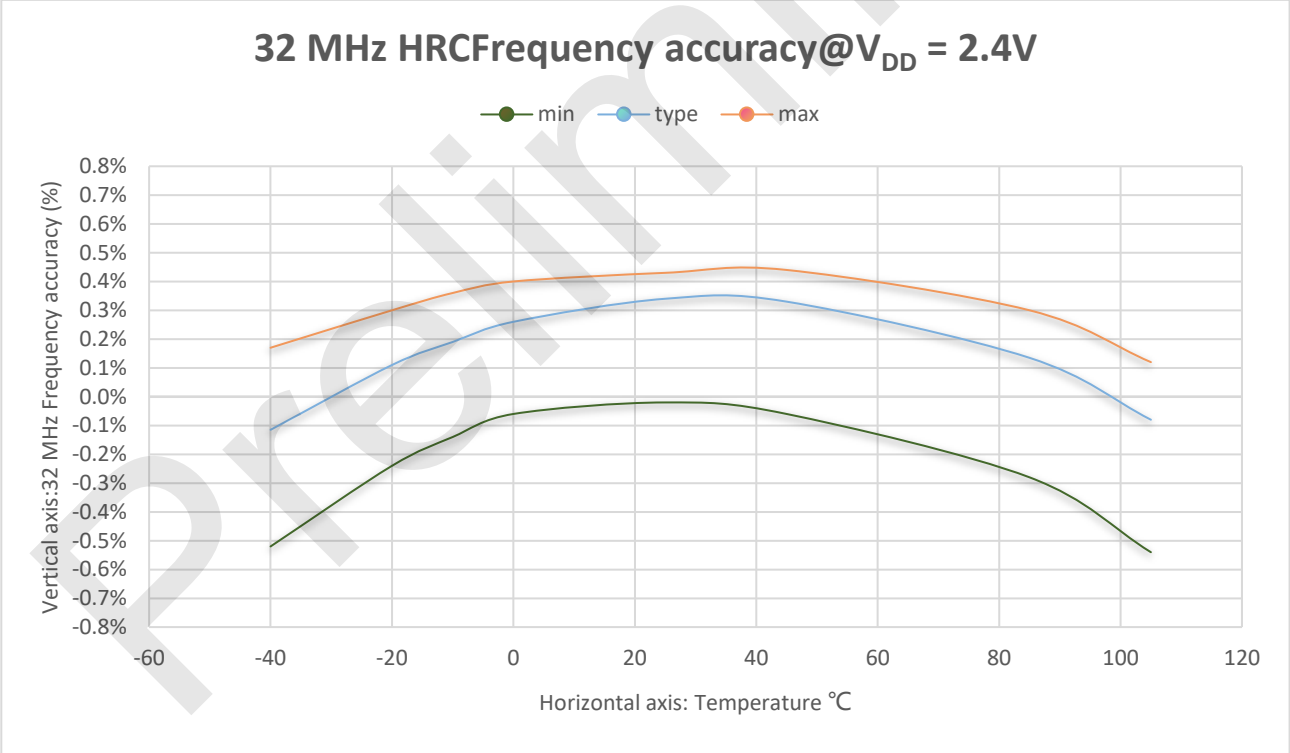
Symbol	Serial Number	DRIV[3:0]	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
	10	1010	Brightness Level 11	-	13.75	-	mA	
	11	1011	Brightness Level 12	-	15.00	-	mA	
	12	1100	Brightness Level 13	-	16.25	-	mA	
	13	1101	Brightness Level 14	-	17.50	-	mA	
	14	1110	Brightness Level 15	-	18.75	-	mA	
	15	1111	Brightness Level 16	-	20.00	-	mA	
	16	CMED=0	/	-	21.25	-	mA	

22.8 AC electrical characteristics

(VDD = 2.4V - 5.5V, TA = 25℃, unless otherwise noted)

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
T_{POR}	Power On Reset Time	-	13	-	ms	
T_{PDW}	Power Down Mode Wake-up Time	-	60	130	μs	
T_{Reset}	Reset Pulse Width	18	-	-	μs	active low
T_{LVR}	LVR debounce time	-	30	-	μs	
f_{HRC}	RC oscillation stability	-1	-	+1	%	V_{DD} = 2.4-5.5 V T_A = -40℃-85℃
		-1.5	-	+1.5	%	V_{DD} = 2.4-5.5 V T_A = -40℃-105℃





22.9 ADC electrical characteristics

(TA = 25℃, unless otherwise noted)

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{AD1}	Power supply voltage 1	2.4	5	5.5	V	Vref = V_{DD} or 1.024 V

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{AD2}	Power supply voltage 2	2.4	5	5.5	V	Vref=2.048 V
V_{AD3}	Power supply voltage 3	2.7	5	5.5	V	Vref=2.4 V
V_{REF1}	Internal reference 1.024V	1.004	1.024	1.044	V	V_{DD} = 2.4-5.5 V
V_{REF2}	Internal reference 2.4V	2.38	2.4	2.42	V	V_{DD} = 2.7-5.5 V
V_{REF3}	Internal reference 2.048V	2.028	2.048	2.068	V	V_{DD} = 2.4-5.5 V
N_R	Accuracy	-	12	-	bit	$GND \le V_{AIN} \le V_{DD}$
V_{AIN}	ADC input voltage	GND	-	V_{DD}	V	
R_{AIN}	ADC input resistance	1	-	-	M	V_{IN} =5 V
I_{lkg_ADC}	ADC input leakage current	-1	-	1	μA	$V_{IN} = V_{AINx}$
I_{ADC1}	ADC conversion current 1	-	1.4	1.8	mA	ADC module enabled V_{DD} = 5 V
I_{ADC2}	ADC conversion current 2	-	1.1	1.5	mA	ADC module enabled V_{DD} = 3.3 V
DNL	Differential nonlinearity error	-	±4	±6	LSB	$V_{REF} = V_{DD}$ = 5 V
INL	Integral nonlinearity error	-	±3	±5	LSB	
E_Z	Offset error	-	±2	±3	LSB	
E_F	Full-scale error	-	±2	±3	LSB	
E_{AD}	Total absolute error	-	-	±6	LSB	
T_{ADC1}	ADC sampling + conversion total time 1	-	1.04	1.3	μs	f_{SYS} = 32 MHz LOWSP[2:0] = 100
T_{ADC2}	ADC sampling + conversion total time 2	-	1.14	1.5	μs	f_{SYS}=32 MHz LOWSP[2:0] = 101
T_{ADC3}	ADC sampling + conversion total time 3	-	1.45	1.9	μs	f_{SYS}=32 MHz LOWSP[2:0] = 110
T_{ADC4}	ADC sampling + conversion total time 4	-	1.95	2.5	μs	f_{SYS}=32 MHz LOWSP[2:0] = 111

22.10 CMP electrical characteristics

(V_{DD} = 5V, T_A = 25℃, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{CM}	Input voltage range	0	-	V_{DD}	V	
V_{OS}	Offset voltage	-	10	30	mV	
V_{HYS}	Comparator voltage hysteresis	-	40	-	mV	
I_{CMP}	Comparator switching current	-	-	100	μA	V_{DD} = 5 V

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
T_{CMP}	Response time	-	-	2	μs	

22.11 OP electrical characteristics

(V_{DD} =5V, T_A = 25℃, unless otherwise specified)

Symbol	Parameter	Minimum Value	Typical Value	Maximum Value	Unit	Condition
V_{OS}	Input offset voltage	-	±3	±10	mV	
V_{CM}	Input common-mode voltage range	0	-	V_{DD}	V	
I_{OP}	OP power supply current	-	300	500	μA	V_{DD} = 5 V
V_{OPO}	OP output voltage	V_{SS}+0.2	-	V_{DD}-0.2	V	V_{DD} = 5 V, load resistance=28.5 kΩ

23 Ordering information

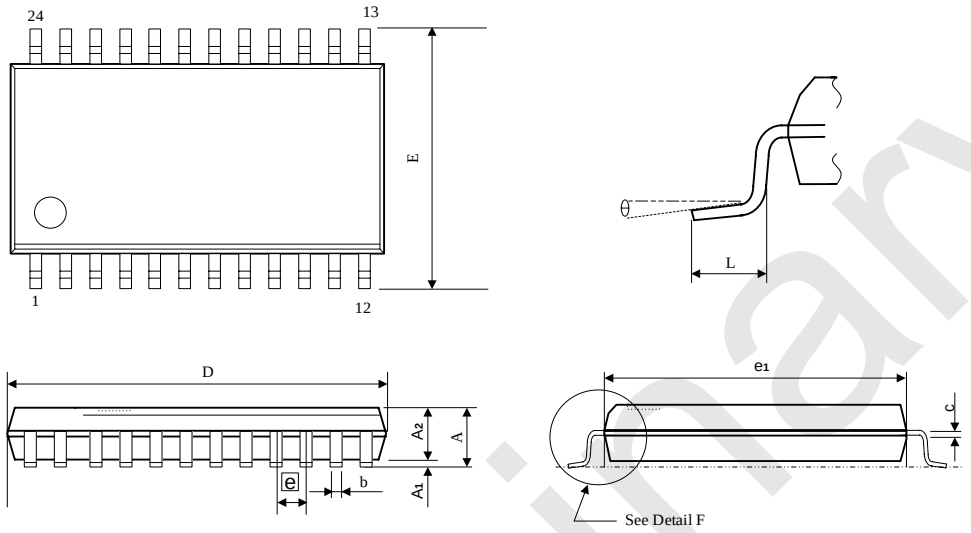
PRODUCT NUMBER	PACKAGE	PACKING
SC92F5319S24U	SSOP24	TUBE
SC92F5319Q24R	QFN24(0404)	TRAY
SC92F5312M20U	SOP20	TUBE
SC92F5312X20U	TSSOP20	TUBE
SC92F5312Q20R	QFN20(0303)	TRAY
SC92F5311M16U	SOP16	TUBE
SC92F5310M08U	SOP8	TUBE

Note: For the mass production status of specific models, please consult SinOne or the distributor's sales representative about sample submission and delivery times before starting development.

24 Package information

SC92F5319S24U

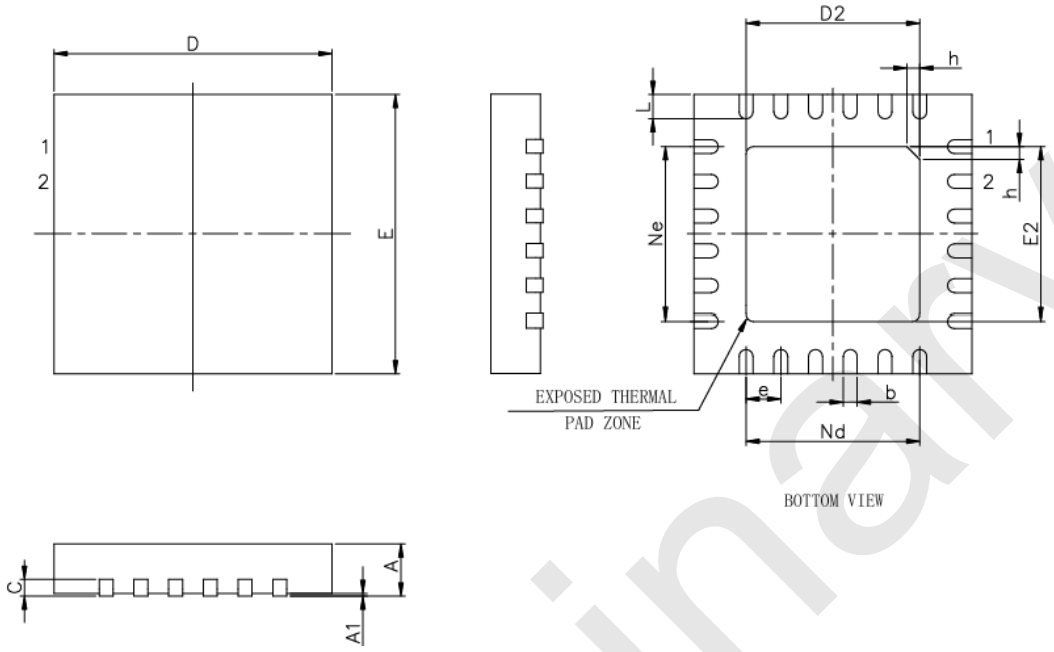
SSOP24 Outline Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A		-	1.750
A1	0.050	-	0.250
A2	-	-	1.550
b	0.200	0.250	0.300
c	0.200 TYP		
D	8.500	8.650	8.800
E	5.900	-	6.200
e1	3.750	3.900	4.050
e	0.635 (BSC)		
L	0.400	-	0.900
θ	0°	-	8°

SC92F5319Q24R

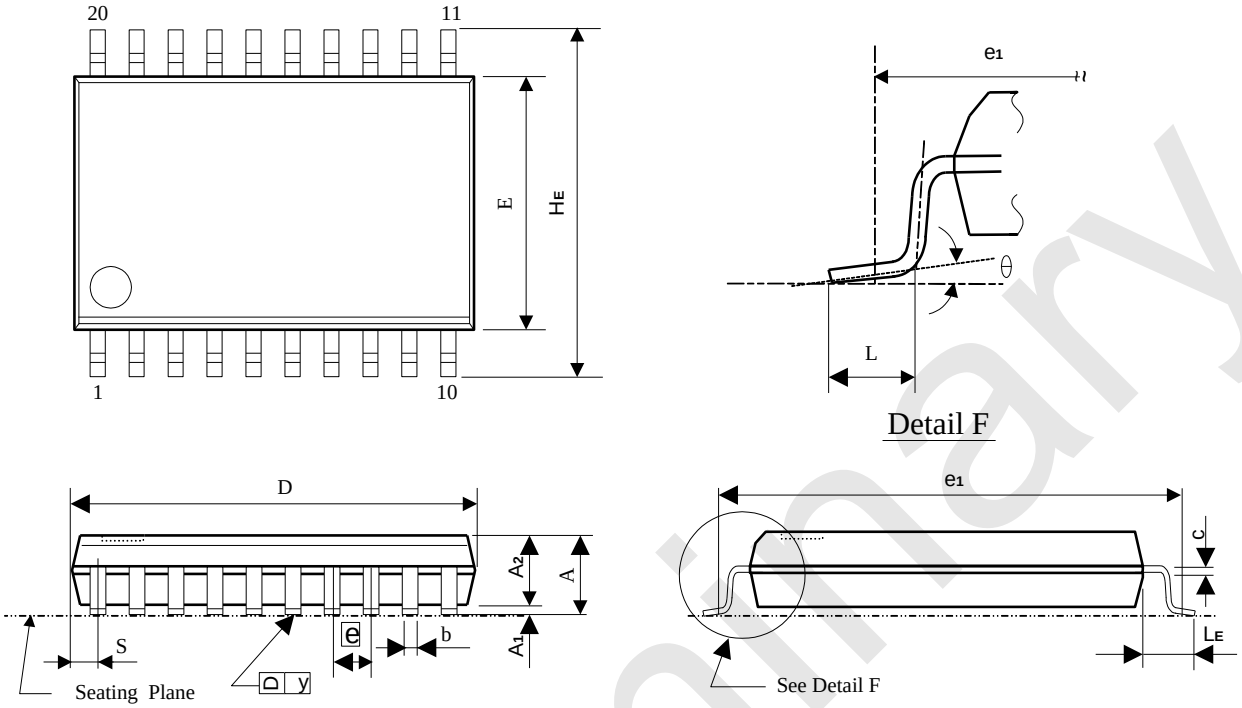
QFN24 (4*4) Outline Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	0.70	0.75	0.80
A1	-	0.02	0.05
c	0.203 REF		
b	0.18	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC		
D2	2.40	2.50	2.60
E2	2.40	2.50	2.60
Nd	2.50 BSC		
Ne	2.50 BSC		
L	0.35	0.40	0.45
h	0.35 REF		

SC92F5312M20U

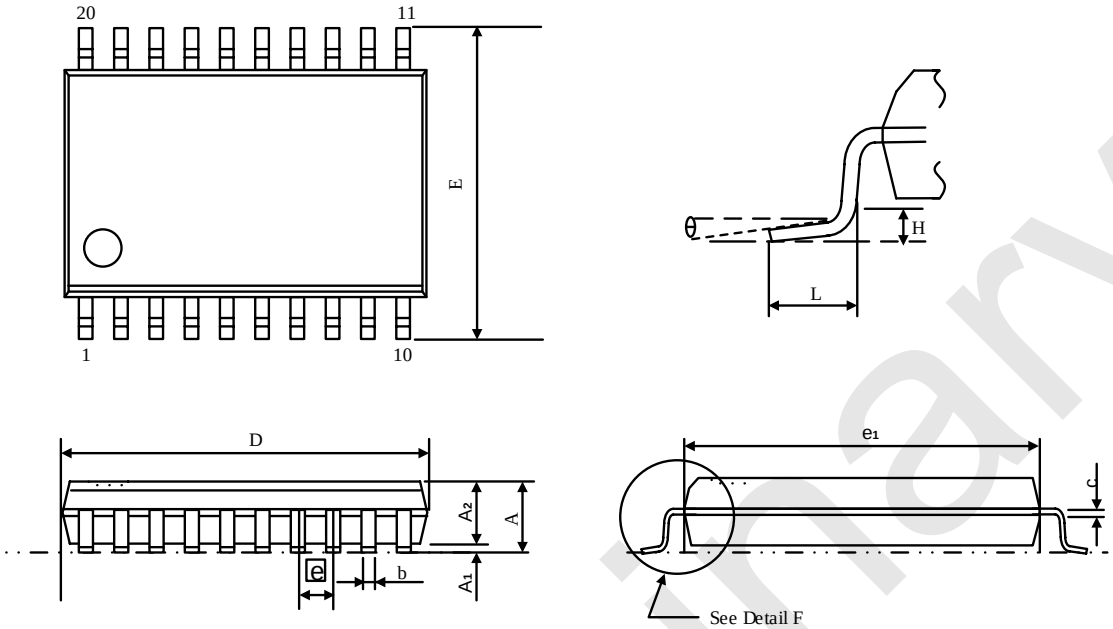
SOP20 (300mil) Outline Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	2.40	2.56	2.65
A1	0.100	0.200	0.300
A2	2.240	2.340	2.440
b	0.35	--	0.47
c	0.25	--	0.31
D	12.60	12.80	13.00
E	7.30	7.50	7.70
HE	10.100	10.300	10.500
e	1.27 (BSC)		
L	0.700	0.850	1.000
LE	1.30	1.40	1.50
θ	0°	-	8°

SC92F5312X20U

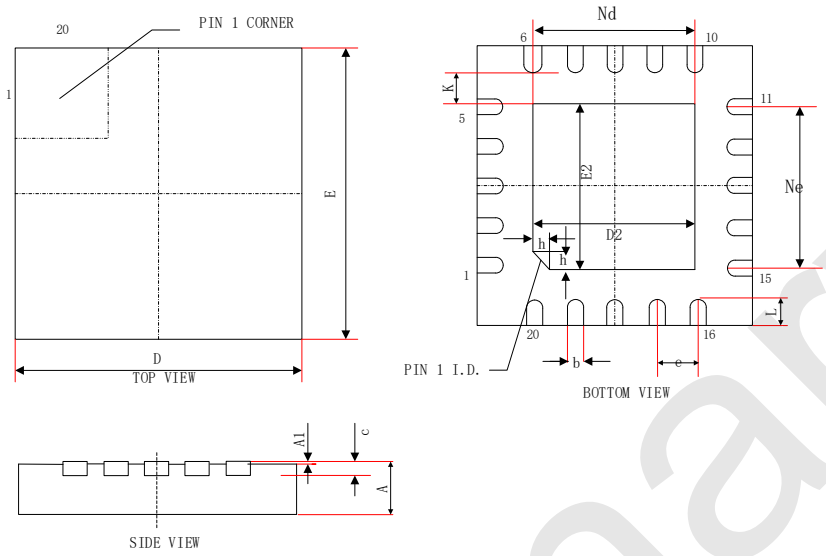
TSSOP20 Outline dimensions (unit: millimeters)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	6.400	-	6.600
E	6.20	-	6.60
e1	4.300	-	4.500
e	0.65 (BSC)		
L	-	-	1.00
θ	0°	-	8°
H	0.05		0.15

SC92F5312Q20R

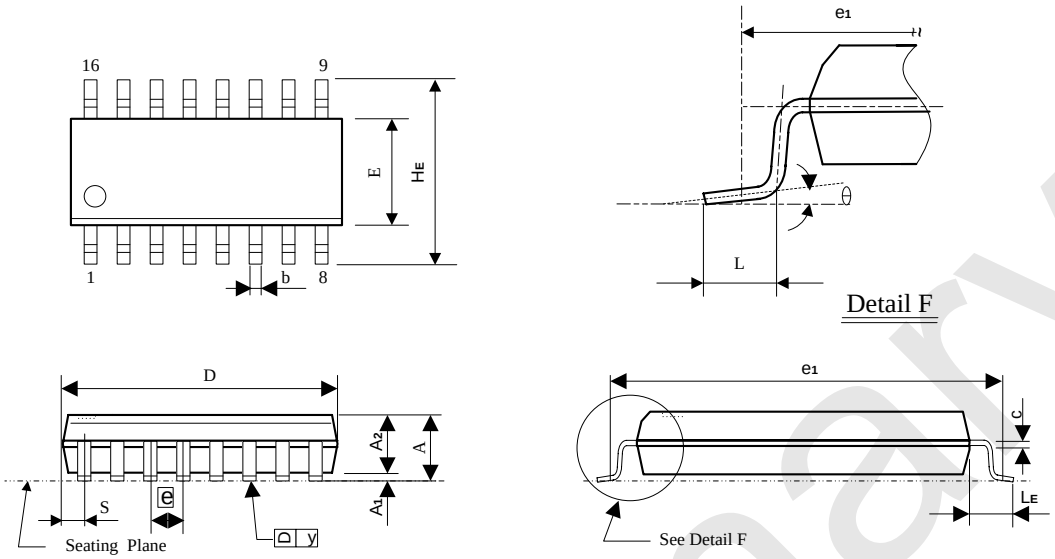
QFN20 L (3*3) Outline dimensions (unit: millimeters)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
c		0.152REF	
D	2.90	3.00	3.10
D2	1.60	1.70	1.80
e		0.40BSC	
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
L	0.25	0.30	0.35
K	0.30	0.35	0.40

SC92F5311M16U

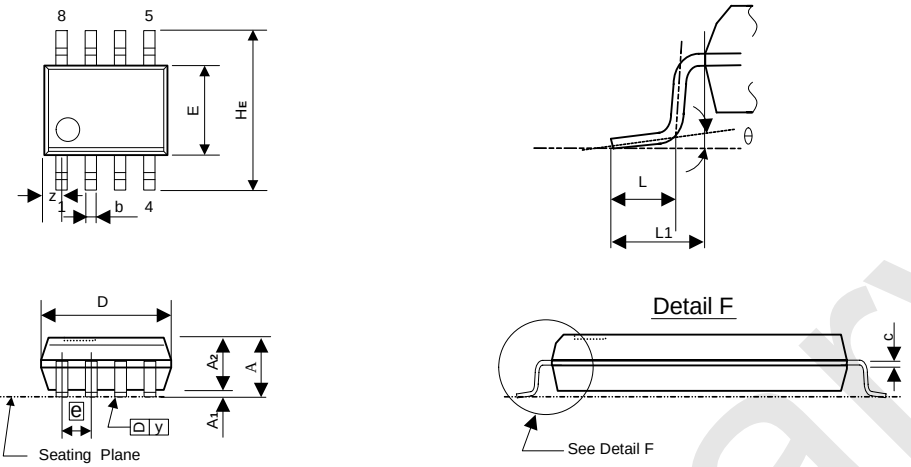
SOP16L (150 mil) Outline dimensions (unit: millimeters)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	1.500	1.625	1.750
A1	0.050	0.1375	0.225
A2	1.30	1.45	1.55
b	0.38	0.43	0.48
c	0.20	0.23	0.26
D	9.70	9.90	10.10
E	3.70	3.90	4.10
HE	5.80	6.00	6.20
e	1.27 (BSC)		
L	0.50	0.65	0.80
LE	0.95	1.05	1.15
θ	0°	-	8°

SC92F5310M08U

SOP8L (150mil) Outline Dimensions (Unit: mm)



Symbol	mm (millimeters)		
	Minimum	Typical	Maximum
A	1.500	1.625	1.750
A**1**	0.100	0.1625	0.225
A**2**	1.30	1.425	1.55
b	0.39	0.435	0.48
c	0.20	0.23	0.26
D	4.70	4.90	5.10
E	3.70	3.90	4.10
HE	5.80	6.00	6.20
e	1.270 (BSC)		
L	0.50	0.65	0.80
L1	0.95	1.05	1.15
θ	0°	-	8°

25 Revision history

Version	Description	Date
V0.1	Initial release	May 26, 2026

Declaration

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